DEVELOPMENT OF AN ELECTROENCEPHALOGRAM (EEG) AMPLIFIER FOR A BRAIN-COMPUTER INTERFACE (BCI)

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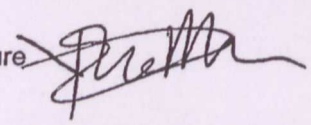
Candidate's Signature  Date 17 FEBRUARY 2006.

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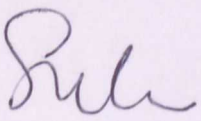
Witness's Signature  Date 21/02/06

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ABSTRACT

A bipolar EEG amplifier developed specifically for use in a brain-computer interface (BCI) is described. An input stage provides very high input impedance to EEG signals. AC coupling is performed in the differential stage to prevent electrode offset voltages from saturating the amplifier when high gain is used. High CMRR is achieved without trimming or component matching. The amplifier is easily modified to amplify other biopotentials. The low power requirement of the amplifier allows it to be powered through the USB connection and is suitable for portable applications.

Four amplifier channels and a DRL circuit were constructed on a board. Two channels were used for amplifying EEG and another two for amplifying EOG and EMG around the throat area for artifact rejection purposes. This amplifier board was used as part of a BCI system that enables the user to select between four prosthetic hand movements and four LEDs representing other devices.

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ABBREVIATIONS

BCI	Brain-computer interface
CMR	Common mode rejection
CMRR	Common mode rejection ratio
DRL	Driven right leg
EEG	Electroencephalogram
EMG	Electromyogram
EOG	Electro-oculogram
FET	Field effect transistor
GBP	Gain bandwidth product
GUI	Graphical user interface
IA	Instrumentation amplifier
LED	Light emitting diode
UM-BCI	University of Malaya brain-computer interface
USB	Universal serial bus

1 INTRODUCTION

1.1 Electroencephalogram

Electroencephalogram (EEG) is a record of electrical brain pattern activities obtained from the difference in potential between two different points on the scalp. The electrical activities recorded from the scalp are due to summed activity of the neurons underlying the recording electrodes. The amplitude of the brain waves may range from 0.5 to 100μV and the frequency may vary from 1 to 40Hz, sometimes higher [1].

There are two types of EEG measurements – monopolar and bipolar. Monopolar measurements are obtained by comparing the potentials from all the electrodes with that from one common reference electrode, while bipolar measurements are obtained by comparing the potentials between pairs of electrodes. The system most commonly used to place electrodes on the scalp is the International Federation 10-20 system, which uses certain anatomical landmarks to standardize placement of EEG electrodes[2].

In the clinical field, EEG is used in diagnosis of brain disease or damage, for example tumors, blood clots, hemorrhage and epilepsy. In the research laboratory, it is used to investigate brain function.

1.2 Brain-Computer Interface

A brain-computer interface (BCI) is defined in [2] as "a communication system in which messages or commands that an individual sends to the external world do not pass through the brain's normal output pathways of peripheral nerves and muscles". Instead, signals produced by brain activity are used to determine the individual's intent.

A BCI is useful for people with disorders that disrupt the neuromuscular channels through which the brain communicates with and controls its external environment. Examples of these disorders are amyotrophic lateral sclerosis (ALS), brainstem stroke, cerebral palsy and spinal cord injury [4]. In severe cases, patients may

lose all voluntary muscle control, including eye movements and respiration and may be completely "locked in" and unable to communicate in any way.

A BCI provides an alternative communication channel for such patients when they can no longer express themselves through speech or action. Presently, BCI systems can provide patients with the ability to answer simple questions, control the environment, and perform slow word-processing [4].

For example, users of the Wadsworth BCI system learn to control electroencephalogram (EEG) signals acquired over the sensorimotor cortex and use that control to move cursors to targets on computer screen. About 80% of users are able to achieve significant control within 2-3 weeks [5].

Another BCI system that also uses EEG signals acquired over the sensorimotor cortex, the Graz BCI, distinguishes between EEG associated with imagination of right or left hand or foot movement. This BCI enables a paralysed user to use hand and foot imagery to control an orthosis that provides hand grasp [6], [7].

Research groups with BCI systems based on EEG rhythms recorded from the scalp over the sensorimotor cortex have demonstrated that the imagination of different movements can be distinguished by using EEG acquired from one or two scalp locations only [8], [9], [10].

The Graz BCI group conducted a field study at an exposition where the BCI system employs two bipolar leads, mounted over the right-hand and foot representation areas. The EEG signals are passed through a bandpass-filter with a passband between 0.5 to 30Hz and sampled at 128Hz. Roughly 93% of the subjects were able to achieve classification accuracy above 60% after two sessions of training [11].

The Wadsworth BCI group uses mu (8-12Hz) and beta (18-26Hz) rhythm amplitudes from one or two scalp locations to allow its user to control cursor movement online. Users achieve accuracies of more than 95% [12].

1.3 University of Malaya brain-computer interface (UM-BCI)

The Department of Biomedical Engineering, University of Malaya is developing a BCI system to enable the user to operate a prosthetic hand. Voluntary motor related EEG recorded from the scalp over the sensorimotor cortex with bipolar EEG leads is used as inputs to the BCI.

A BCI box contains the signal acquisition unit and the universal serial bus (USB) controller. The signal acquisition unit, consisting of an EEG amplifier and an analog to digital converter (ADC), acquires EEG from the scalp and digitizes it. Digitised EEG data is sent to a computer through the USB.

The computer processes the signal to extract specific features and classify them according to the respective motor imagery. The computer then determines the corresponding hand movement and outputs an instruction for the hand movement through the USB to the hand controller. The hand controller receives the computer output and controls the hand to perform the selected movement.

Figure 1.1 shows the components of the UM-BCI system.

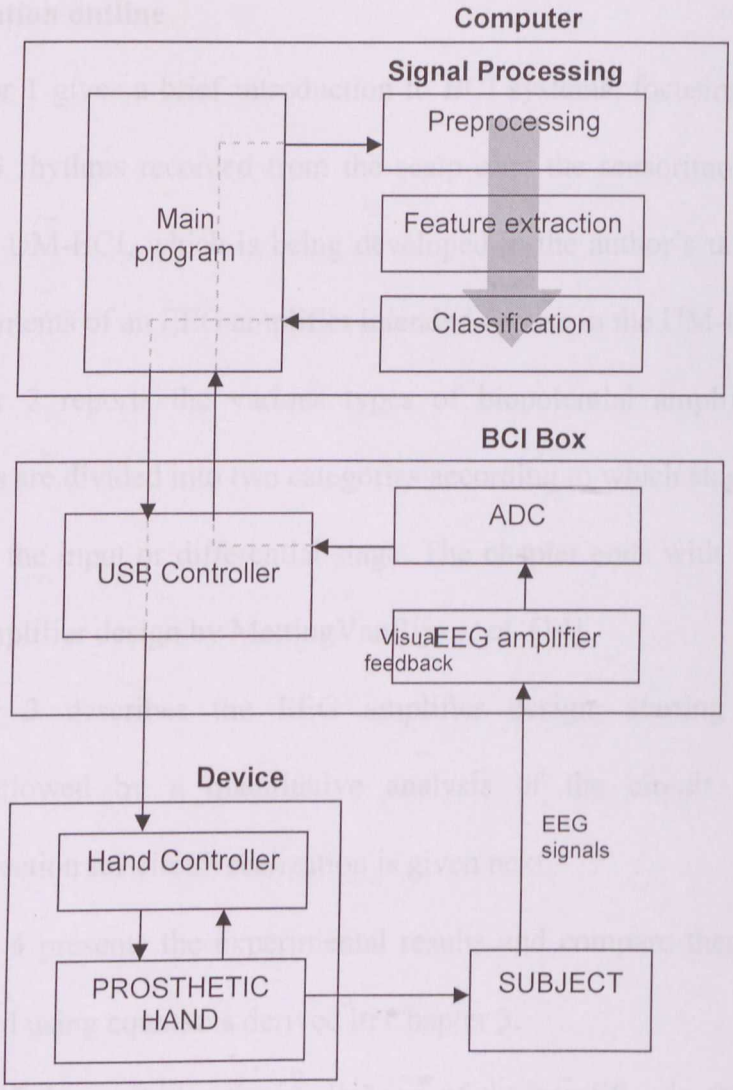


Figure 1.1: Block diagram showing the components of the UM-BCI.

1.4 Objective

The objective of this project is to develop an EEG amplifier for use in the UM-BCI. The requirements are:

- The amplifier design should consume little power so that it can be powered by the USB. The USB standard for low power bus powered device is 100mA. This 100mA will be shared with the USB controller and ADC.
- The amplifier gain and bandwidth should be easy to modify so that it can be changed to amplify other bio-potential signals like electro-oculogram (EOG) and electromyogram (EMG).
- The design should not rely highly on component matching to achieve high CMRR.

1.5 Dissertation outline

Chapter 1 gives a brief introduction to BCI systems, focusing on BCI systems based on EEG rhythms recorded from the scalp over the sensorimotor cortex. It also introduces the UM-BCI, which is being developed in the author's university, and lists out the requirements of an EEG amplifier intended for use in the UM-BCI.

Chapter 2 reports the various types of biopotential amplifier designs. The various designs are divided into two categories according to which stage the ac-coupling is implanted – the input or differential stage. The chapter ends with a highlight of the biopotential amplifier design by MettingVanRijn *et al.* [14].

Chapter 3 describes the EEG amplifier design, starting with a general description, followed by a quantitative analysis of the circuit. IC and passive components selection for circuit realization is given next.

Chapter 4 presents the experimental results and compare them with the target values calculated using equations derived in Chapter 3.

Chapter 5 demonstrates the application of the amplifier in the UM-BCI in an actual training session.

Chapter 6 is contains the conclusion of this report.

2. LITERATURE REVIEW

2.1 DC electrode offset voltages

Electrodes and the electrolyte paste convert ionic currents in the body to electronic currents that can be measured by the amplifier. Oxidation and reduction reactions occurring at the electrode-electrolyte interface forms a layer of charge at the interface, causing an electrode potential to develop across the interface. The difference in electrode potential between two electrodes is a dc voltage called the electrode offset potential [13].

The presence of dc electrode offset potentials poses a problem in the measurement of bio-potential signals that requires high amplification, for example EEG signals. Electrode offset potential can be of the order of several millivolts, which is very much higher in magnitude than EEG signals (1 to 100μV). When high gain is used in a dc-coupled amplifier, the amplifier output will saturate. To prevent this, amplifier voltage gain is limited to moderate values (around 30dB) when using dc-coupled input stage amplifiers. The necessary gain is provided by subsequent ac-coupled differential stage [14]. Another way is to implement ac-coupling in the input stage.

2.2 AC coupled input stage amplifier designs

The most basic ac-coupled amplifier is an inverting amplifier with a capacitor placed between the input signal and the amplifier input resistor, as shown in Figure 2.1 [15]. The input impedance depends on R_1 and this is not desirable as the very high input impedance of the op amp is not taken advantage of and the maximum input impedance of the amplifier depends on the largest resistor value available, which is usually 100MΩ.

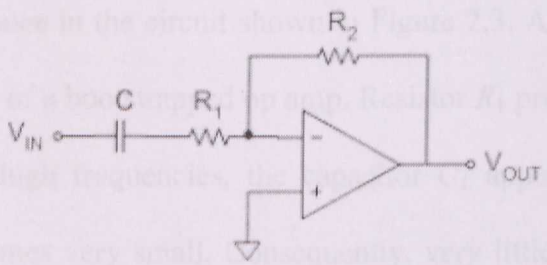


Figure 2.1: An inverting ac-coupled amplifier.

A non-inverting ac-coupled non-inverting amplifier is shown in Figure 2.2. R_{BIAS} is needed to provide a path for bias currents to flow from the op amp non-inverting terminal. However, putting a resistor between the op amp terminal and ground effectively reduces the input impedance of the amplifier to R_{BIAS}. Again, the input impedance is limited to the largest resistor value available. Most of the time, the resistor value of R_{BIAS} is made to be equal to $R_1R_2/(R_1+R_2)$ to cancel out the effects of op amp bias currents.

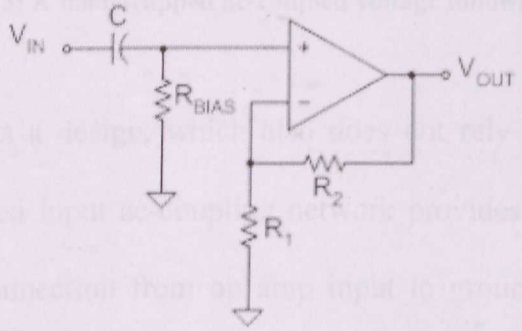


Figure 2.2: A non-inverting ac-coupled amplifier.

This small R_{BIAS} value (compared to the op amp input impedance) may cause amplifier common-mode rejection (CMR) degradation due to electrode-skin impedance differences. Coupling capacitor, C mismatches further degrade the CMR. Even if the circuit is trimmed for maximum CMR, maintaining performance over temperature can be a problem.

Figure 2.3 shows the bootstrapped ac-coupled voltage follower proposed in [16]. It solves the problem of having to rely on unusually large bias resistors to maintain high

amplifier input impedance in the circuit shown in Figure 2.3. A capacitor, C_2 is placed in series with the input of a bootstrapped op amp. Resistor R_1 provided a path for the op amp bias current. At high frequencies, the capacitor C_1 appears as a short and the voltage across R_1 becomes very small. Consequently, very little current flows through R_1 and very high input impedance is achieved for high frequency signals without having to use unusually high value resistors.

The gain can be increased by replacing the short between the inverting pin and output with a resistor [15].

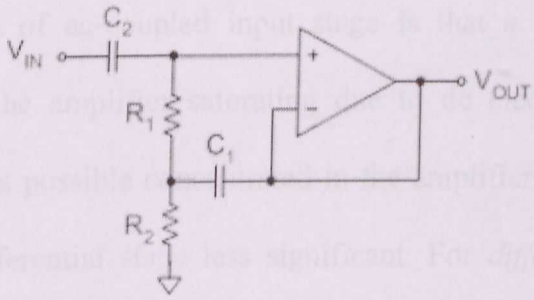


Figure 2.3: A bootstrapped ac-coupled voltage follower in [16].

Figure 2.4 shows a design, which also does not rely on unusually large bias resistors [17]. A balanced input ac-coupling network provides a path for op amp bias currents without any connection from op amp input to ground, thus preserving high common-mode rejection ratio (CMRR). Differential signals are ac-coupled and common mode voltages are dc coupled. When a common mode voltage appears at its inputs, no currents flow through the network and hence no common mode voltage appears at the op amp inputs. Ideally, the circuit has infinite CMRR. However, the amplifier input impedance depends on R_1, and it must be as high as possible to avoid loading effects on the input signal.

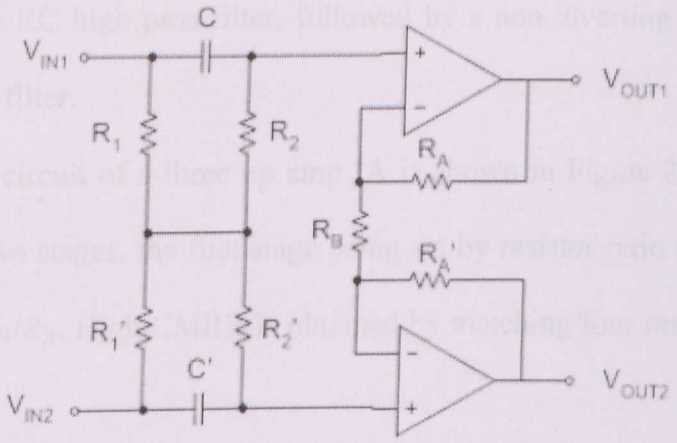


Figure 2.4: A balanced input ac-coupling network proposed in [17]

The advantages of ac-coupled input stage is that a very high gain can be implemented without the amplifier saturating due to dc electrode offset potentials. Having as much gain as possible concentrated in the amplifier first stage makes noise from the following differential stage less significant. For *difference-input-difference-output* circuits [17], high gains at the input stage also increases amplifier CMRR because the common mode gain is limited to unity regardless of differential mode gains.

However, the ac-coupled input stage designs reviewed rely a lot on component matching to preserve the CMRR of its differential stage. This makes circuit realization expensive and difficult. Furthermore, component values may drift over time resulting in CMRR degradation.

2.3 AC coupled differential stage amplifier designs

Ac coupling can also be performed by a differential stage which follows a dc coupled input stage. Instrumentation amplifiers (IA), either two or three op amp, are usually used to *differentiate* the two input signals.

An example of a biopotential amplifier preamplifier is given in [18]. Signals from electrodes are dc coupled to an IA with a gain of only 25 to prevent op amp saturation due to electrode offset voltages up to 300mV. The output of the IA is sent

through a passive RC high pass filter, followed by a non-inverting amplifier that also acts as a low pass filter.

The basic circuit of a three op amp IA is shown in Figure 2.5 [19]. IA gain is implemented in two stages, the first stage being set by resistor ratio $(R_1+R_2)/R_1$ and the second stage by R_B/R_A. High CMRR is obtained by matching four resistors: R_A, R_A', R_B and R_B'.

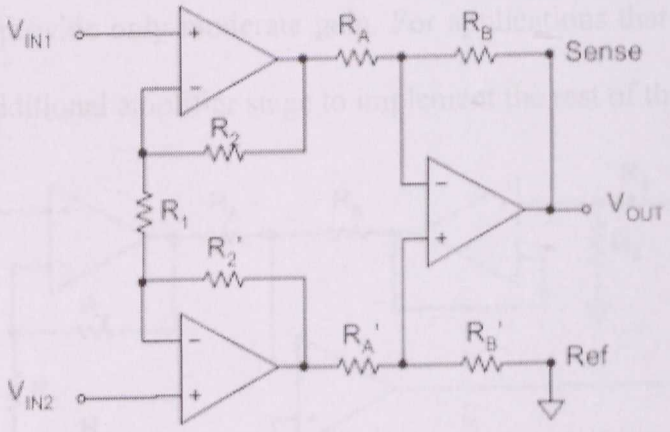


Figure 2.5: Basic three op amp instrumentation amplifier.

Feeding back the integrated output voltage (V_{OUT}) to the reference input (*Ref*) suppresses input dc differential voltage. However, the differential dc input voltage range is limited by the maximum output voltage of the integrator op amp. This range can be increased by either reducing the gain in the first stage or reducing the resistor ratio R_B/R_A but this also means reducing the amplifier gain to values below the required gain for EEG amplifiers in order to accommodate a wider input dc differential voltage range.

Smit *et al.* [20] proposed selecting an initial low gain for the IA, then feeding the sense input (labeled '*Sense*' in Figure 2.5) of the IA with a fraction of the output voltage to implement the rest of the required gain. Directly connecting the sense input to the resistors that form a potential divider will degrade the CMRR. Hence, a monolithic current feedback IA with on-chip voltage to current converter sense-inputs (AMP01) was used to preserve its CMRR even when resistors are connected directly to the sense input.

If a wider selection of op amps is preferable, a buffer op amp can be added between the sense input and the resistors [21], as shown in Figure 2.6. The gain of the differential stage is realized by the resistor ratio $(R_3+R_4)/R_3$. The drawback of this circuit is that the high pass cutoff frequency is equal to $(R_3+R_4)/R_3$ x $(1/RC)$. In order to achieve low cutoff frequency (<0.5Hz) and high gain, either the capacitor, C or the resistor value, R has to be very large and this will increase the size of the PCB. As a result, the IA can provide only moderate gain. For applications that require high gain, there must be an additional amplifier stage to implement the rest of the gain.

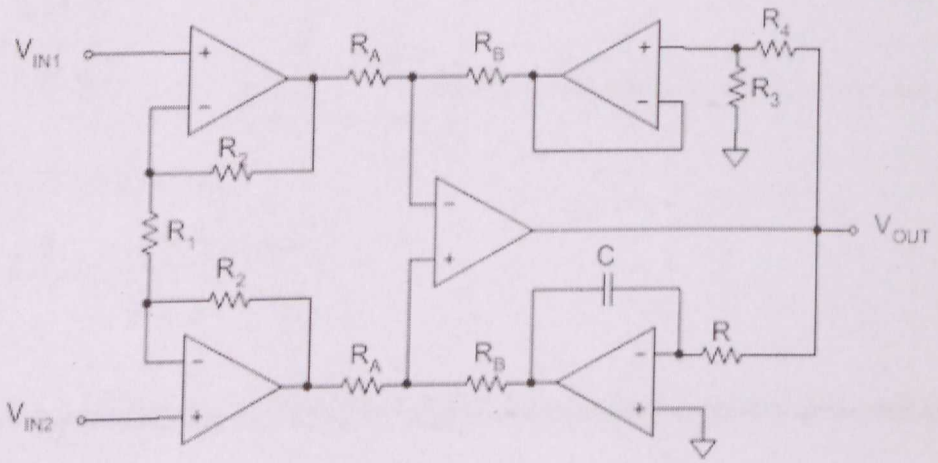


Figure 2.6: Amplifier proposed in [21].

2.4 Biopotential amplifier design by MettingVanRijn *et al.*

MettingVanRijn *et al.* [14] presented a biopotential amplifier design that uses fewer parts than conventional designs by using a two op amp instrumentation amplifier instead of a three op amp instrumentation amplifier. It has the advantage of reduced dimensions and lower power consumption.

Integrated output voltage is fed back to the sense input instead of the reference input, as shown in Figure 2.7. AMP2 acts as both an integrator and buffer for the resistive potential divider formed by R_5 and R_6. For low gains, the second integrator (AMP3) is not required but at high gains, a significant offset equal to the input offset voltage of AMP2 multiplied by the gain setting resistor ratio $(R_5+R_6)/R_5$ will appear in

the output. The second integrator is added to remove this offset in the output. The high pass cutoff frequency is set with R_A, C_A, R_B and C_A. Compared with the design proposed in [21], very large capacitor or resistor values are not needed to achieve the desired cutoff frequency.

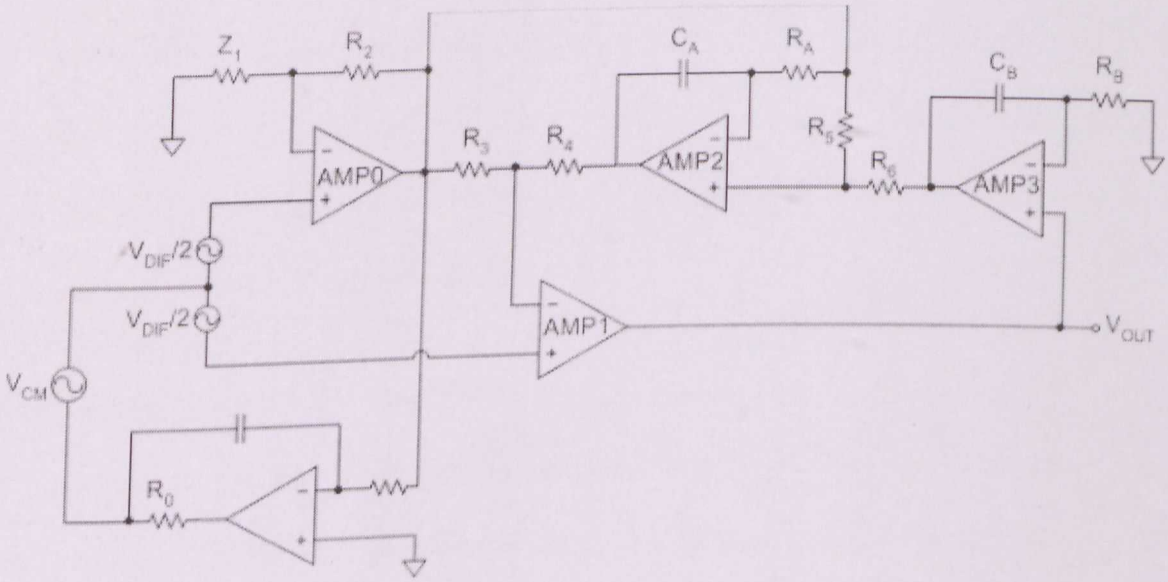


Figure 2.7: Biopotential amplifier with two op amp instrumentation amplifier presented by Metting *et al.* [14].

The limited gain-bandwidth product (GBP) of the op amp and high amplifier gain are taken advantage of to provide the required low pass response for the amplifier. If an oversampling ADC is used to digitize the amplifier output, the very high sampling rate will allow for a wide filter transition band. The first order low pass frequency response should be adequate to reduce aliasing errors in the digitized signal and no additional op amps will be needed to construct a low pass filter. The low pass response can also be set by placing a capacitor in parallel with R_6.

For low differential gains, high CMRR is achieved by matching impedances

$$\frac{Z_1}{R_2} = \frac{R_4R_5 + R_3R_6 + R_4R_6}{R_3R_5}$$

For high differential gains, as needed in EEG amplifiers, R_2 is shorted because the high differential gain made up for the mismatch and the CMRR will not be significantly degraded.

3 EEG AMPLIFIER DESIGN

3.1 Research methodology

The research approach to this work is by first reviewing existing bio-potential amplifier designs. Then, a circuit is designed by drawing ideas from the amplifiers reviewed. An analysis of the amplifier is done to calculate resistor and capacitor values as well as to aid in selection of the suitable op amp ICs. An actual EEG amplifier PCB is built and experiments and tests are conducted to evaluate the functionality and performance of EEG amplifier. Finally, the EEG amplifier is integrated with the BCI system to ensure that it can be used in a BCI.

3.2 The proposed EEG amplifier

The dc rejection circuit employing negative feedback of the integrated output presented by MettingVanRijn *et al.* [14] is adapted to prevent amplifier saturation due to high gains and electrode offset voltages. This dc rejection circuit has the advantage of not relying on matched capacitor values to preserve CMRR and not needing very high values of capacitors or resistors.

The two op amp instrumentation amplifier (IA) is replaced by a three op amp IA to achieve constant high CMR ratio regardless of gain. The three op amp IA also provides better CMR at high frequencies compared with two op amp IAs due to the symmetrical inverting and non-inverting gain paths in the three op amp IA [19]. Figure 3.1 shows the proposed EEG amplifier.

The input stage is constructed using low input bias current op amp and resistors. Resistance matching in the input stage is not so critical because effects of mismatch in resistors R_2 and R_2' will just cause a gain error without affecting the CMRR of the circuit [15].

The resistors in the differential stage, however, must be accurately matched to ensure high CMRR. The common mode gain is zero if the resistor ratios R_4/R_3 equals

R_4'/R_3'. Hence, monolithic difference amplifier ICs with on-chip trimmed resistors can be used to construct the differential stage and high CMRR can be achieved easily.

A driven-right-leg (DRL) circuit is used to provide a return path for bias currents of the input stage op amps and to reduce common mode interference in the signal [22], [23], [24]. Without a bias current return path, the currents will charge stray capacitances and the inputs will float to a potential which exceeds the common-mode range of the op amp, causing the op amp to saturate.

Resistors R_{FB} averages the voltage between electrodes to obtain the common mode voltage, which is amplified by an inverting integrator and sent back to the body through the DRL electrode. A series resistor R_O limits the current to the patient in the event of a fault to 10μA.

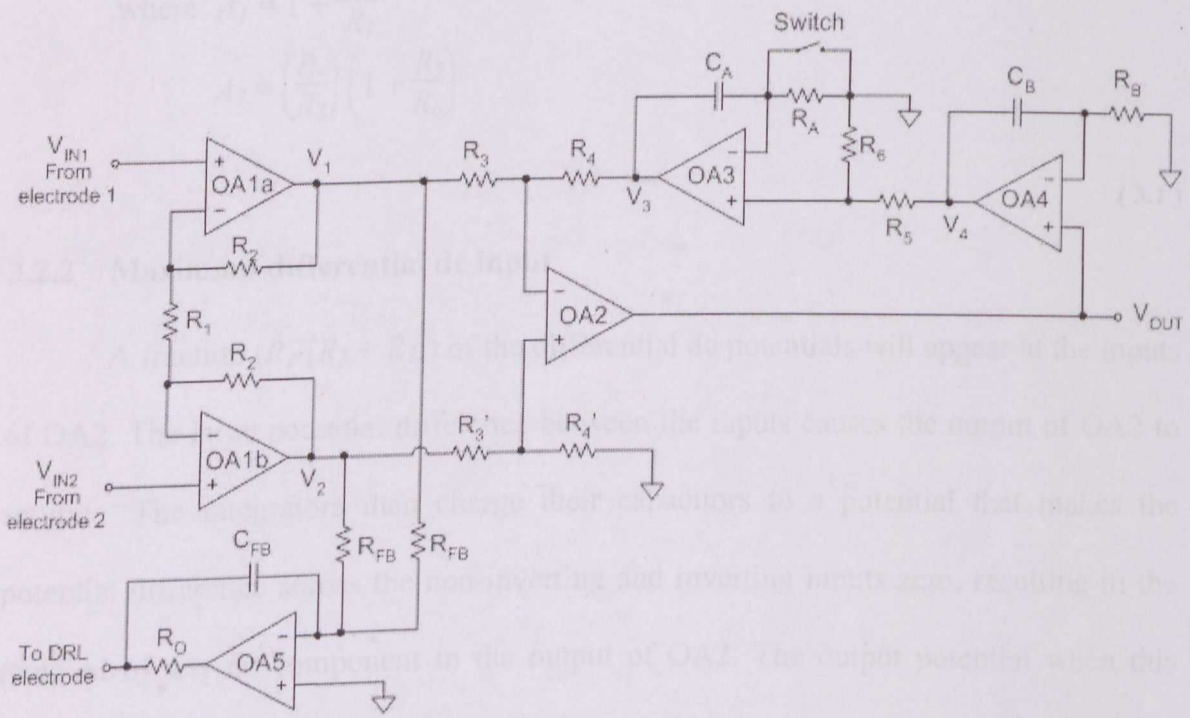


Figure 3.1: The proposed EEG amplifier.

3.2.1 Differential gain

Total amplifier gain is realized in two stages. The first stage, or input stage, is the a dc-coupled *difference input, difference output amplifier*, which amplifies the differential signals by A_1 but limits the gain of common mode signals to unity. The

second stage, or differential stage, is a difference amplifier with a portion of the output, V_{OUT} fed back to its negative input. It amplifies the differential signal by A_2 and ideally, the common mode gain is zero.

The amplifier differential transfer function is given by equation (A.3) in the Appendix (Section A.1):

$$V_{OUT} = \left(1 + \frac{2R_2}{R_1}\right)\left(\frac{R_4}{R_3}\right)\left(1 + \frac{R_5}{R_6}\right)\left(\frac{sR_AC_A}{1 + sR_AC_A}\right)\left(\frac{sR_BC_B}{1 + sR_BC_B}\right) V_{DM}$$

For high frequencies, where $sR_AC_A >> 1$ and $sR_BC_B >> 1$, the equation can be simplified to:

$$V_{OUT} = A_1 A_2 \quad V_{DM}$$

$$\text{where} \quad A_1 = 1 + \frac{2R_2}{R_1}$$

$$A_2 = \left(\frac{R_4}{R_3}\right)\left(1 + \frac{R_5}{R_6}\right)$$

(3.1)

3.2.2 Maximum differential dc input

A fraction ($R_4/[R_3 + R_4]$) of the differential dc potentials will appear at the inputs of OA2. The large potential difference between the inputs causes the output of OA2 to saturate. The integrators then charge their capacitors to a potential that makes the potential difference across the non-inverting and inverting inputs zero, resulting in the removal of any dc component in the output of OA2. The output potential when this happens is:

$$V_3 = (V_2 - V_1)(R_4 / R_3)$$

However, V_3 is limited to the maximum output of OA3 and this limits the maximum differential dc input of the differential stage to

$$(V_2 - V_1)_{(max)} = V_{3\,(max)}\,(R_3 / R_4)$$

The input stage gain causes the differential dc input to appear as A_1 x V_{DM} to the differential stage. Hence, The maximum differential dc input of the amplifier, $V_{DM(max)}$ is:

$$V_{DM(max)} = V_{3(max)} (R_3 / R_4) / A_1 \tag{3.2}$$

3.2.3 Lower cutoff frequency

The integrators in the feedback loop produce a 2nd order high pass response in the amplifier transfer function. By letting $R_A = R_B = R$ and $C_A = C_B = C$, the transfer function of the amplifier is:

$$\frac{V_{OUT}}{V_{DM}} = A_1 A_2 \left(\frac{sRC}{1 + sRC}\right)^2$$

Substituting $s = jw$, the magnitude of V_{OUT}/V_{DM} is

$$|V_{OUT}/V_{DM}(jw)| = A_1 A_2 \frac{(wRC)^2}{1 + (wRC)^2}$$

At high frequencies($(wRC)^2 >> 1$), $|V_{OUT}/V_{DM}(jw)|$ is maximum and is equal to A_1A_2. At the –3dB frequency, w_{LC}, $|V_{OUT}/V_{DM}(jw)|$ is $1/\sqrt{2}$ times the maximum magnitude. Hence,

$$A_1A_2 \frac{(w_{LC}RC)^2}{1 + (w_{LC}RC)^2} = \frac{1}{\sqrt{2}} A_1A_2$$

Rearranging the above equation shows that the lower –3dB frequency is:

$$w_{HP} = 1.554/RC, \text{ or } f_{HP} = 0.2473/RC \tag{3.3}$$

The natural baseline recovery of the amplifier is very slow, much slower than a simple dc reject RC circuit, because only a small fraction (R_6/ [R_5+R_6]) of the V_4 appears at the non-inverting input of OA3 and across R_B. Hence, only a small current charges capacitor C_B and it takes a long time for V_3 to reach the '*dc-canceling*' voltage. To solve this problem, a '*normally open*' switch is placed across resistor R_B. When the

switch closes, a short appears across R_B and large current charges the capacitor, C_B quickly to return the baseline to 0V.

3.2.4 Upper cutoff frequency

Since the differential stage gain, A_2 is considerably large, the limited GBP of the op amp will produce a low pass response. The upper –3dB frequency frequency,

$$f_{UC} \approx f_{t2}\left(\frac{R_3}{R_3 + R_4}\right)\left(\frac{R_6}{R_5 + R_6}\right)$$

where f_{t2} is the unity gain bandwidth of OA2 (The derivation is included in the Appendix - Section A.2).

The bandwidth specification given in the datasheets of monolithic difference amplifiers is assumed to refer to $f_{t2}\left(\frac{R_3}{R_3 + R_4}\right)$ (Section A.3 in the Appendix shows the working to obtain the relationship between difference amplifier small signal bandwidth and op amp unity gain bandwidth). Therefore, the upper cutoff frequency of the amplifier when monolithic difference amplifier is used is

$$f_{UC} \approx f_{SSB2}\left(\frac{R_6}{R_5 + R_6}\right) \qquad (3.4)$$

where f_{SSB2} is the closed-loop small signal bandwidth of the difference amplifier used.

When low gain value is used, resistor ratio $R_6/(R_5+R_6)$ produces an upper –3dB frequency which may be very much higher than the required cutoff frequency. The upper –3dB frequency can be lowered by adding a capacitor in parallel with R_5 [14]. Denoting this capacitor as C_5 and replacing R_5 in equation (A.3) with $Z_5 = R_5/(sR_5C_5+1)$, we get:

$$V_{OUT} = \left(1 + \frac{2R_2}{R_1}\right)\left(\frac{R_3}{R_4}\right)\left(1 + \frac{R_5 / R_6}{1 + sR_5C_5}\right)\left(\frac{1 + sR_AC_A}{sR_AC_A}\right)\left(\frac{1 + sR_BC_B}{sR_BC_B}\right) V_{DM}$$

If the resistor ratio R_5/R_6 is very much larger than 1, the upper –3dB frequency can be approximated as

$$f_{UC} \approx 1/(2\pi R_5 C_5) \tag{3.5}$$

3.3 Components selection

3.3.1 IC selection

Dual low noise, FET-input op amp by (OPA2130) with low bias currents (10pA maximum) is used as OA1a and b. The maximum input bias current is very much lower than that the IEC601-1:1988 dc patient auxiliary current limit of 10μA [25].

OA2 and four matched resistors (R_3, R_3', R_4 and R_4') are implemented using INA132, a unity gain monolithic difference amplifier. The CMRR of OA1a and b (minimum 90dB) is higher than the CMRR of the difference amplifier (minimum 76 dB) and this will increase the overall amplifier CMRR.

The integrator op amps, OA3 and OA4 use OPA2735, which are CMOS op amps with very low offset voltage plus near-zero drift over time and temperature and rail-to-rail output.

All ICs used are able to operate with a supply voltage of ±5V. 0.1μF multilayer ceramic capacitors are placed across each IC power supply pins to decouple high frequency noise in the power supplies.

A summary of the op amp specifications is shown in Table 3.1.

Table 3.1: Summary of op amp specifications.

	Texas Instruments OPA2130	Texas Instruments INA132	Texas Instruments OPA2735
Ib (pA) *max*	10	-	200
Input offset voltage (mV) *max*	1	0.5	0.005
CMRR (dB) *min*	90	76	115
Input voltage noise at 100Hz (nV/√Hz)	18	-	150

Output voltage range when supply voltage is ±5V (V)	-3.8 to 3	-4.75 to 4	-4.95 to 4.95
Open loop gain (dB) *min*	120	-	115
GBP (MHz)	1	0.3	1.5
Slew rate (V/μs) *typ*	2	0.1	1.5
Quiescent current per channel (mA) *typ*	0.53	0.155	0.75

3.3.2 Passives selection

All resistors used in the amplifier circuit are from the Philips RC02H series of precision chip resistors, with resistance tolerance of 1% and temperature coefficient of less than 100ppm/°C.

3.3.2.1 Input stage gain, A_1

Rearranging equation (3.2),

$$A_1 = \frac{R_3}{R_4} \frac{V_{3(\max)}}{V_{DM(\max)}}$$

The R_3 / R_4 ratio is 1 and the output of OA3, V_3, can swing from -4.95V to +4.95V. To obtain a $V_{DM(max)}$ of at least 300mV, the gain, A_1 should be less or equal to 16.5.

The gain, A_1 is set by resistors R_2 and R_1 (equation (3.1)). The resistor values must be relatively small to minimize the effects of bias current [15].

R_1 of 1kΩ and R_2 of 6.8kΩ will set A_1 to 14.6.

3.3.2.2 Differential stage gain, A_2

A total gain of 50 000 will amplify a 100μV_{P-P} signal to 5V_{P-P}. The input stage provides 14.6 gain. To achieve a target gain of 50 000, the differential stage must provide a gain of 3424.7. R_6 of 1kΩ and R_5 of 3.3MΩ will set A_2 to 3301. The total amplifier gain is (A_1 x A_2) = 48195.

3.3.2.3 Common mode rejection ratio

The minimum CMRR of INA132 is 76dB. Amplifier CMRR is further increased with input stage gain. The first stage limits A_{CMI} to unity even with mismatched R_2 resistor values. Then, CMRR contribution from the input stage gain is

$CMRR_{A1} = 20 \log_{10} (14.6 / 1) = 23.$

The total CMRR will be at least (23 + 76) = 99dB, which is above the minimum CMRR of 80dB required of biopotential amplifiers.

3.3.2.4 Lower cutoff frequency

Using 100nF capacitors and 4.7MΩ resistors, the high pass cutoff frequency is:

$f_{LC} = 1.554/ (2\pi \times 4.7 \times 10^{6} \times 100 \times 10^{-9}) = 0.5Hz$

Panasonic metallised polyphenylene sulphide (PPS) film capacitors (ECHU series), with tolerance of 2%, are used in the integrator because of their small dielectric leakage current.

4 EEG AMPLIFIER SPECIFICATIONS

4.1 Test equipment

The tests were carried out using a function generator, a digital oscilloscope, a digital multi-meter and a custom made circuit to test for differential ac and dc input range (Figure 4.1). Power was provided using two PP3 9V battery and ±5V voltage regulators.

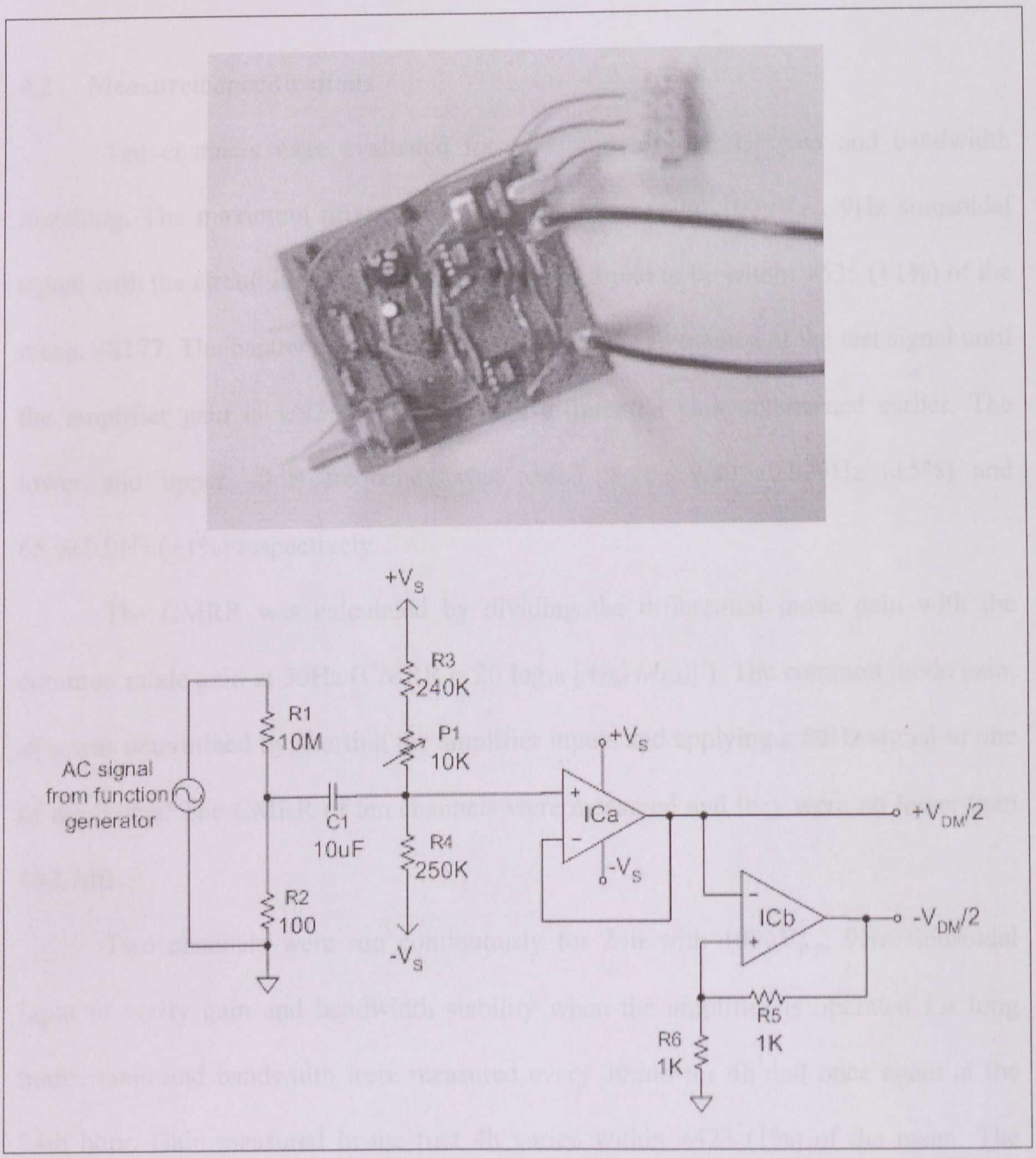


Figure 4.1: A photograph (top) and schematic (bottom) of the circuit used to test differential dc and ac input range.

The circuit in Figure 4.1 was used to produce two signals of opposite polarities, $+V_{DM}/2$ and $-V_{DM}/2$. AC signal from the function generator is reduced to microvolts by the potential divider formed by R_1 and R_2. The reduced ac signal is ac coupled by C_1 and fed to the non-inverting input of dual op amp *ICa*. This input is dc biased by the resistor R_3, R_4 and potentiometer P_1. Varying P_1 will shift the dc bias level. The output of *ICa* is sent to a unity gain inverting amplifier *ICb*. The outputs of *ICa* and *ICb*, $+V_{DM}/2$ and $-V_{DM}/2$, are applied to the amplifier inputs.

4.2 Measured specifications

Ten channels were evaluated for maximum differential gain and bandwidth matching. The maximum differential gain was tested using $100\mu V_{p-p}$, 9Hz sinusoidal signal with the circuit in Figure 4.1. The gain was found to be within ±535 (±1%) of the mean, 48177. The bandwidth was tested by varying the frequency of the test signal until the amplifier gain is $1/\sqrt{2}$ of its maximum differential gain determined earlier. The lower and upper –3dB frequency was tested to be 0.509±0.023Hz (±5%) and 65.9±0.9Hz (±1%) respectively.

The CMRR was calculated by dividing the differential mode gain with the common mode gain at 50Hz (CMRR = $20 \log_{10} [A_{DM} / A_{CM}]$). The common mode gain, A_{CM} was determined by shorting the amplifier inputs and applying a 50Hz signal to one of the inputs. The CMRR of ten channels were measured and they were no lower then 102.7dB.

Two channels were run continuously for 24h with $100\mu V_{p-p}$, 9Hz sinusoidal input to verify gain and bandwidth stability when the amplifier is operated for long hours. Gain and bandwidth were measured every 30min for 4h and once again at the 24th hour. Gain measured in the first 4h varied within ±423 (1%) of the mean. The lower and upper bandwidth varied within ±0.027Hz (5%) and ±2Hz (3%) of the mean.

Gain and bandwidth measured at the 24th hour were found to be within the range of gain values obtained in the first 4h.

Gain and bandwidth measured on 5 different days were also compared to verify their repeatability. Gain, lower and higher bandwidth varied within ±0.7%, ±1.7% and ±1.4% of the mean.

Similar effort to verify stability and repeatability of CMRR over time was done on two channels. The channels were run continuously for 24h and the CMRRs were measured every 30min for 4h and once at the 24th hour. The maximum deviation of values obtained in the first 4h was 1.5 dB below and 8.6dB above the mean. CMRR measured at the 24th hour were within the range of values obtained in the first 4h. CMRR measured in 5 different days showed little variation (1.9dB below and 1.3dB above the mean).

The differential dc input range was tested with a 100uVp-p, 10Hz ac signal on an increasing differential dc signal. The differential ac input range was measured by increasing the magnitude of the 10Hz signal applied at the amplifier inputs until signal 'clipping' was observed on the oscilloscope screen.

The power consumption was also measured by applying a 100uVp-p, 10Hz ac signal to the amplifier inputs. Currents flowing through the power supply terminals (+5V, 0V and –5V) were determined by placing the digital multimeter in series with the wires supplying power to the board. It was observed that very little current flows through the 0V terminal and the currents flowing in and out of the +5V and –5V terminal were almost equal. This shows that most of the current flows in from the +5V terminal and out through the –5V terminal. Hence, the power consumption is calculated multiplying the current flowing through either the +5V or –5V terminal with 5 – (-5) = 10V.

The intrinsic noise level (r.t.i.) was approximated by determining the voltage range on the oscilloscope screen which contains nearly all of the signal. The rms noise is estimated by dividing this range by 6. This method assumes the noise follows a Gaussian distribution and has an accuracy of ±20% [26]. Figure 4.2 shows the signal at the amplifier output when both the inputs were shorted. Most of the noise signal falls within ±40mV.

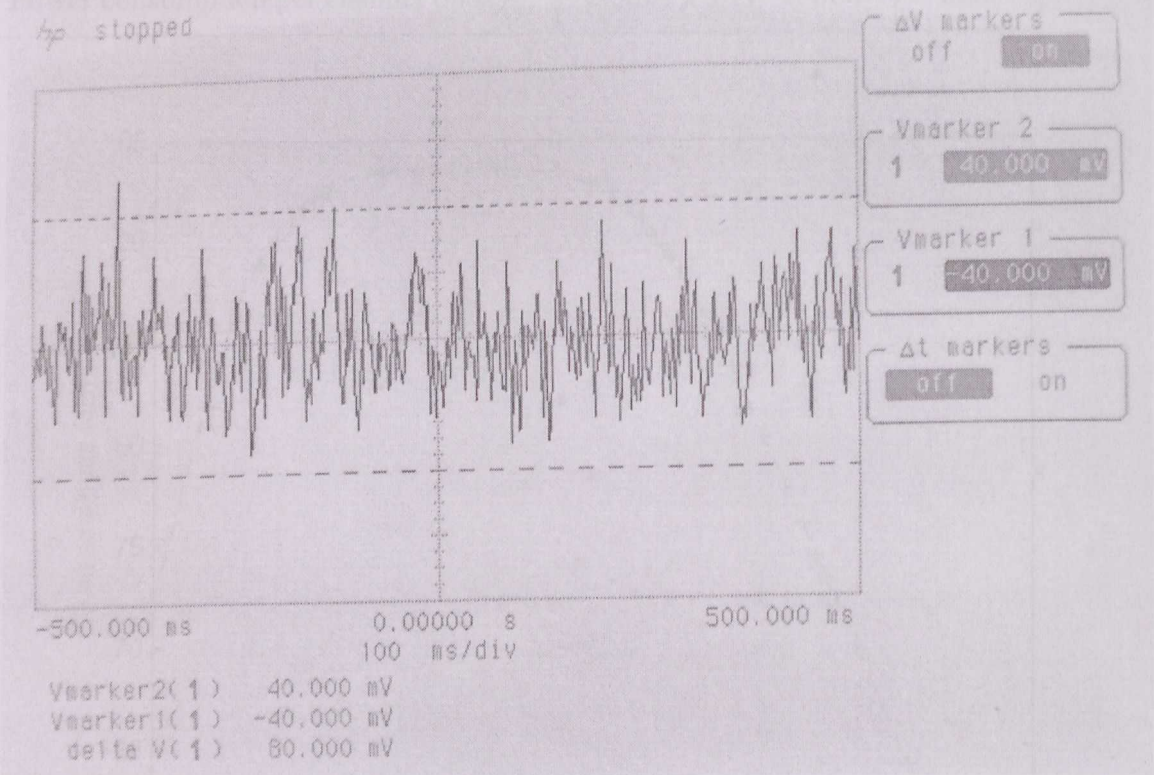


Figure 4.2: A photograph of the oscilloscope screen showing the noise level at the amplifier output when both the amplifier inputs were shorted together.

The experimental data is included in Appendix D. Summarised experimental results are tabulated in Table 4.1. Figure 4.3 shows a plot of experimental gain magnitude vs. frequency. The dotted line shows simulated bandpass response with a passband gain of 48177, 0.509Hz second order HPF and 65.9Hz first order LPF. The '+' markers are the experimental values.

Table 4.1: Summary of measured EEG amplifier specifications.

Parameters	Measured values	Units
Gain *(mean)*	48177	
Bandwidth(-3dB) (*mean*)	0.509 to 65.9	Hz
Differential ac input range (*min*)	171	μV_{p-p}
Differential dc input range (*min*)	±340, -341.3 to 340.8	mV
CMRR at 50Hz (*min*)	102.7	dB
Intrinsic noise (rti) (*max*)	0.28	μV_{rms}
Power consumption per channel (*max*)	2.5mA x 10V=25mW	mW

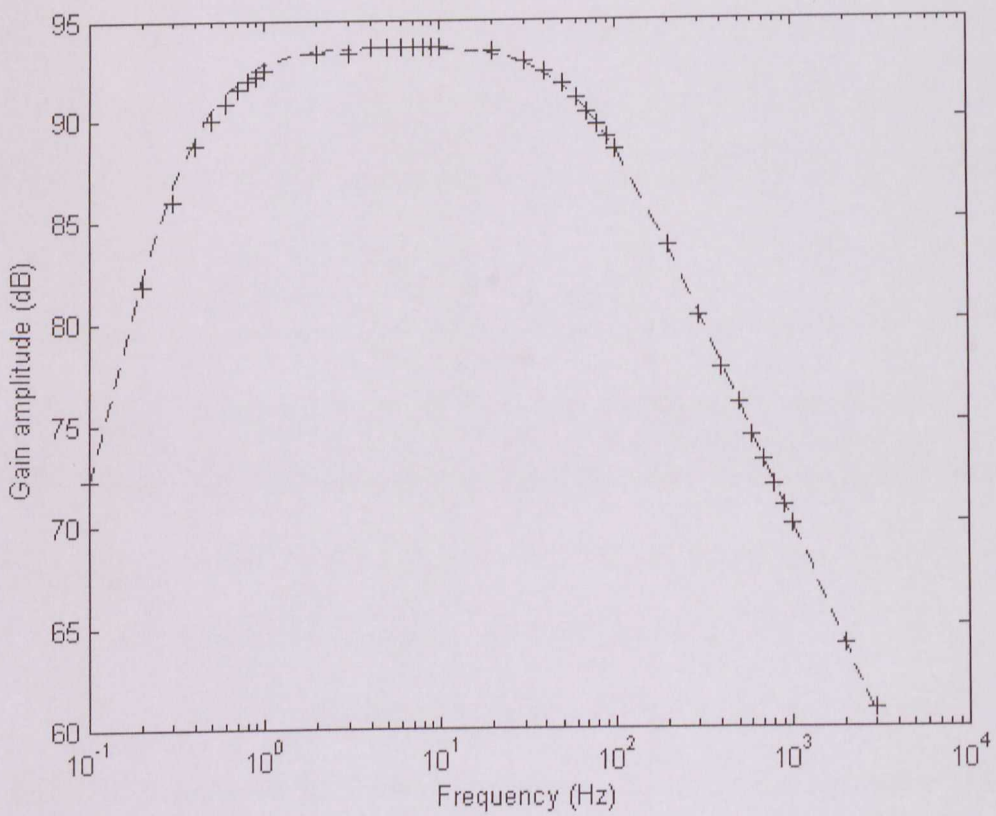


Figure 4.3: Plot of the gain magnitude vs. frequency for an EEG amplifier channel.

4.3 Measured vs. target specifications

The measured differential passband gain, lower cutoff frequency, differential input range and CMRR values agree with target values calculated in section 3.3. However, the measured upper cutoff frequency (65.9Hz) falls short of the 91Hz cutoff frequency calculated using equation (3.4). This may be because the op amp used in the monolithic difference amplifier is assumed to be of the compensated type when deriving

the equation. Still, equation (3.4) can be used to roughly estimate the amplifier low pass frequency response given the differential stage gain, A_2 and the difference amplifier small signal bandwidth, f_{SSB2}. If a higher gain or –3dB frequency is desired, adjustments can be made by replacing INA132 with another difference amplifier IC with larger (small signal) bandwidth and then adding C_5 to set the desired –3dB frequency.

5 INTEGRATION TO UM-BCI

5.1 Interfacing to the ADC

The ADC used in the UM-BCI is Analog Devices AD7716. It is a sigma delta ADC set to sample at 524kS/s (Samples per second) with an oversampling ratio of 3910:1. The high oversampling ratio renders a first order low pass response adequate to prevent aliasing errors in the ADC output.

The ADC has an on-chip digital low pass filter that attenuates high frequency components and decimates these samples to provide data at an output rate of 256Hz. As a result, the frequency response of the ADC output will be similar to that of a cascade with two filters – a 65.9Hz first order analog low pass filter provided by the EEG amplifier, and a 67Hz $sinc^3$ response digital low pass filter provided by the ADC. The resultant response has a –3dB frequency at 45Hz, which is acceptable because it is still above 40Hz, which is the upper limit of the frequency band of interest.

The ADC input has a small sampling capacitor in parallel with an input resistance greater than 1GΩ. The analog signal appearing at the inputs of the ADC is produced directly from the output of OA2 and thus, the output resistance is very small and will not have significant effect on the ADC gain error.

A photograph of the USB data acquisition board which has two AD7716 ADC chip and a USB controller (not shown in photograph, mounted on the other side of the board) is shown in Figure 5.1.

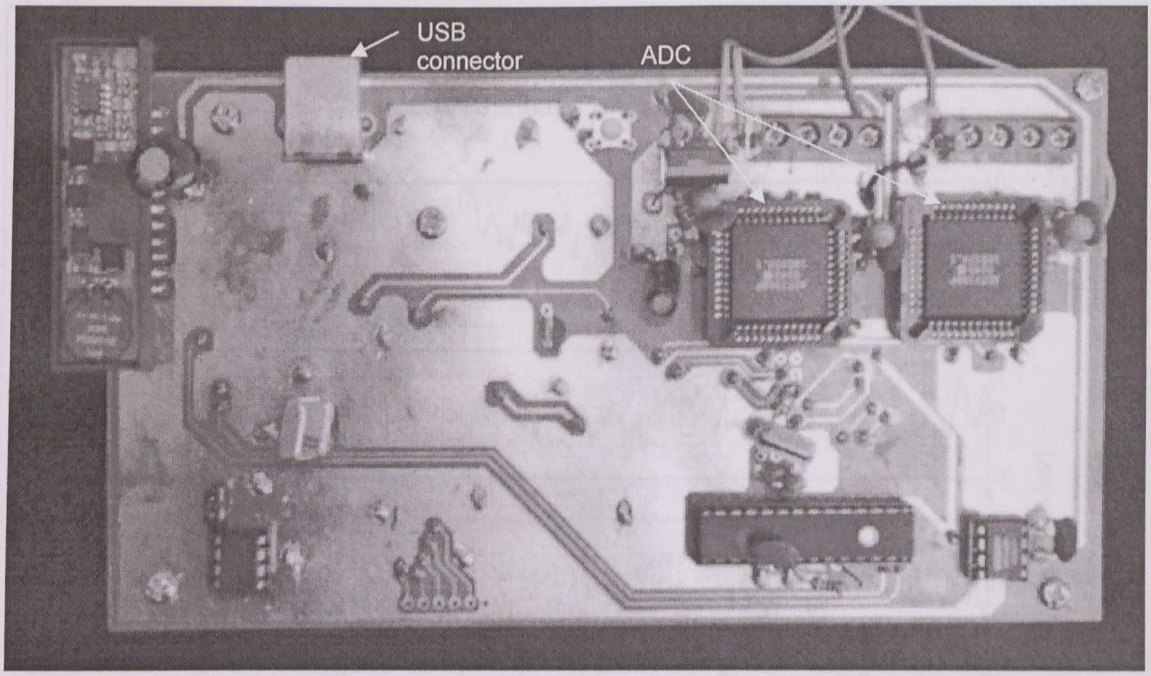


Figure 5.1: A photograph of the USB data acquisition board.

5.2 Application in UM-BCI

The EEG amplifier was used in the UM-BCI to acquire bipolar EEG signals using 10mm diameter, scalp electrodes by TECA, Oxford Instruments Medical.

The top figure in Figure 5.2 shows a segment of the EEG extracted from the recording during a training session where the subject has to imagine left hand and foot movement. The EEG signal was acquired from bipolar electrode pairs on the *Cz-aCz* and *C4-pC4* 10-20 system locations. The bottom figure shows the averaged power spectral plot of EEG signals for the entire session. The subject exhibits a stronger beta rhythm (18 to 26Hz component) in her EEG acquired from the *Cz-aCz* electrode pair when she was performing foot motor imagery than left hand motor imagery. This characteristic was used to enable the subject to select options in a GUI (graphical user interface). The options are four prosthetic hand movements and four LEDs representing other devices.

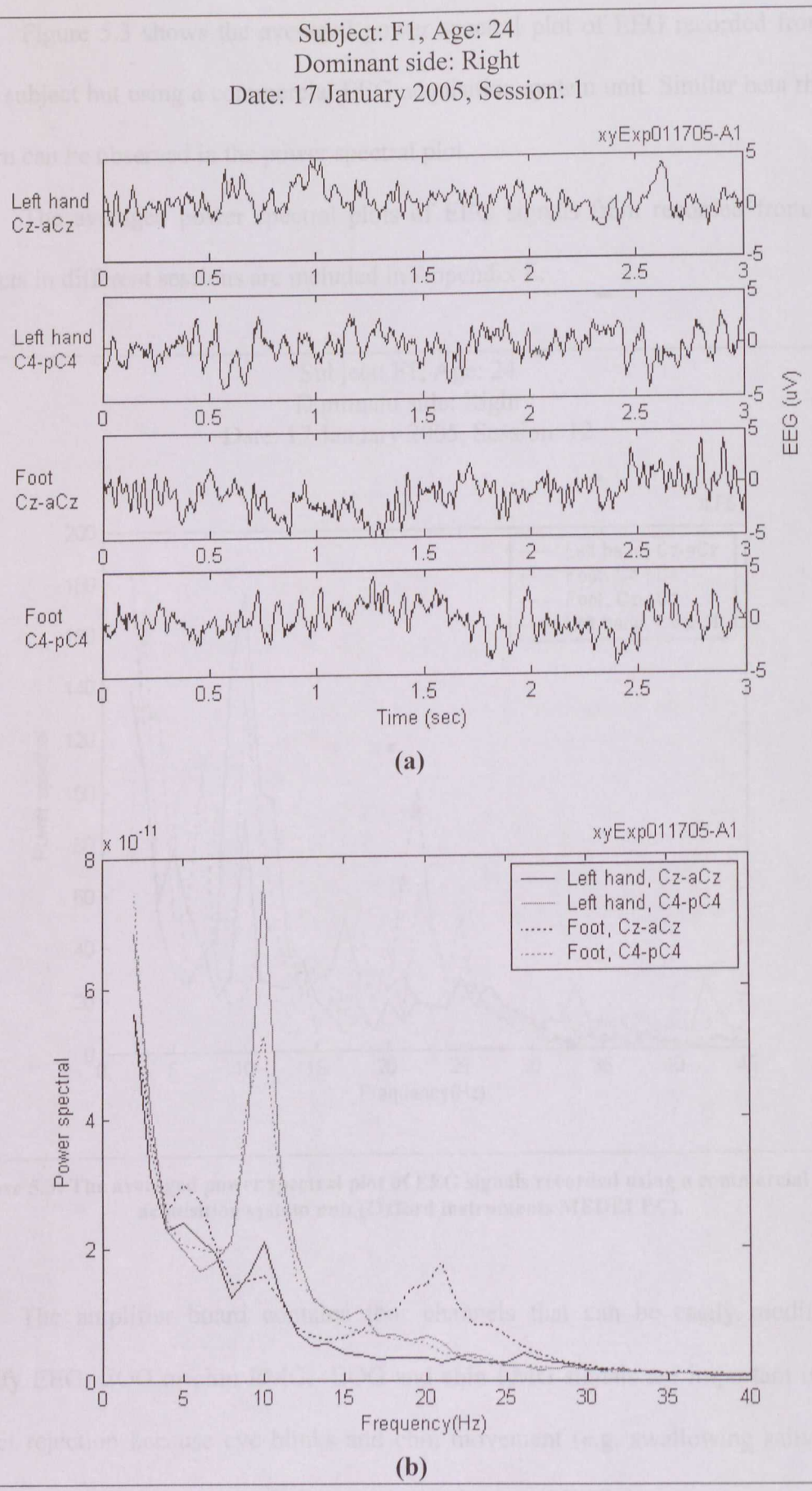


Figure 5.2: (a) A segment of the EEG acquired; (b) The averaged power spectral plot of the EEG signals during a BCI training session using the amplifier built.

Figure 5.3 shows the averaged power spectral plot of EEG recorded from the same subject but using a commercial EEG acquisition system unit. Similar beta rhythm pattern can be observed in the power spectral plot.

The averaged power spectral plots of EEG signals from recorded from other subjects in different sessions are included in Appendix E.

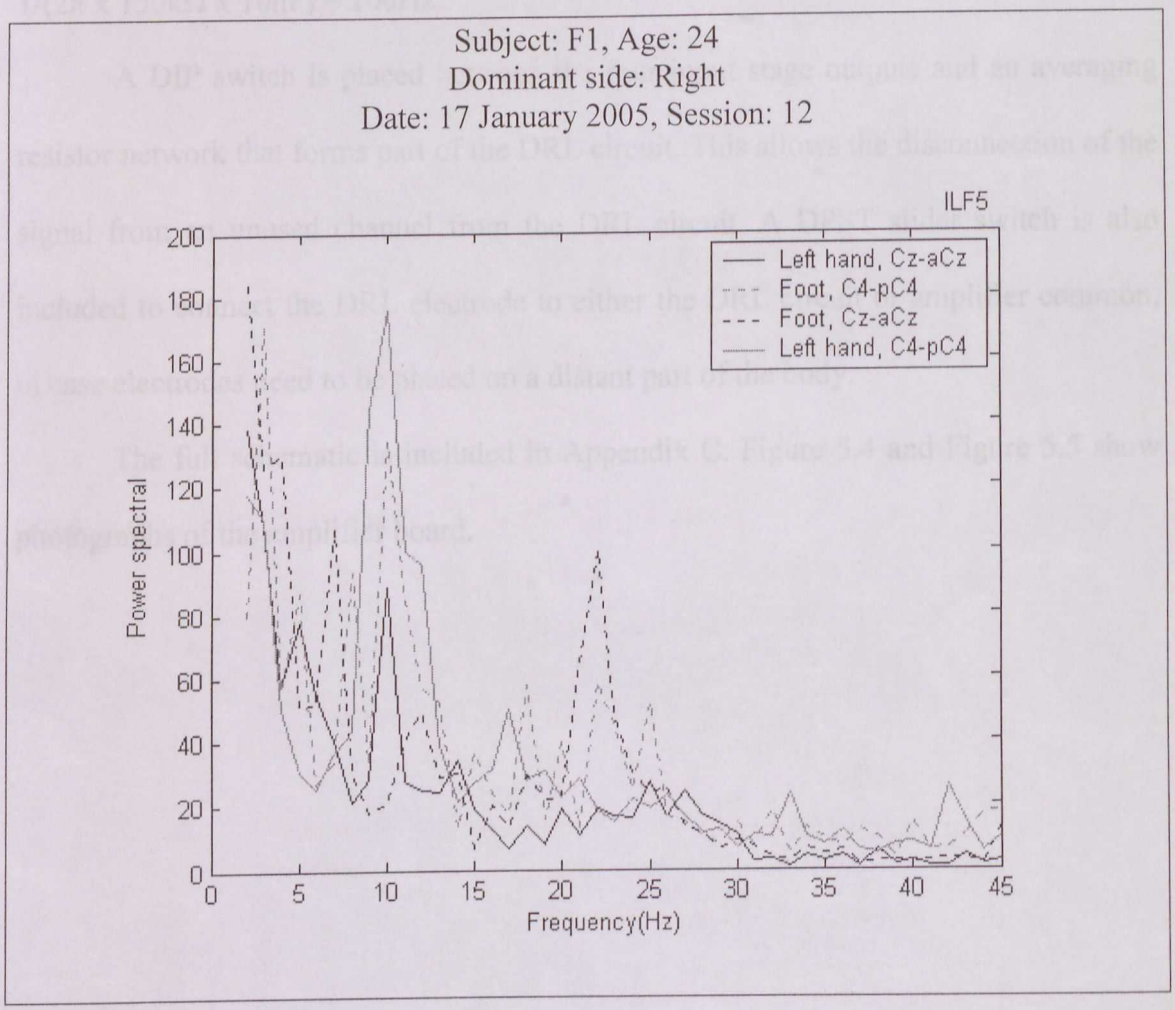


Figure 5.3: The averaged power spectral plot of EEG signals recorded using a commercial EEG acquisition system unit (Oxford instruments MEDELEC).

The amplifier board contains four channels that can be easily modified to amplify EEG, EOG or chin EMG. EOG and chin EMG signals are important in EEG artifact rejection because eye blinks and chin movement (e.g. swallowing saliva) can affect the EEG signals and might be mistaken to be actual EEG features.

The modifications are made by changing the R_5 resistor value and by adding a capacitor (C_5) in parallel to R_5 to set the appropriate gain and low pass –3dB frequency.

The CMRR and differential dc input range would not be affected by changes in gain and bandwidth.

Currently, two EEG channels are used in each BCI training session. Two other channels are used to acquire EOG and chin EMG signals. The EOG and EMG channels are set to gains of 14.6 x (150kΩ + 1kΩ)/1kΩ = 2205 and low pass –3dB frequency of $1/(2\pi \times 150k\Omega \times 10nF) = 106Hz$.

A DIP switch is placed between the four input stage outputs and an averaging resistor network that forms part of the DRL circuit. This allows the disconnection of the signal from an unused channel from the DRL circuit. A DPST slider switch is also included to connect the DRL electrode to either the DRL circuit or amplifier common, in case electrodes need to be placed on a distant part of the body.

The full schematic is included in Appendix C. Figure 5.4 and Figure 5.5 show photographs of the amplifier board.

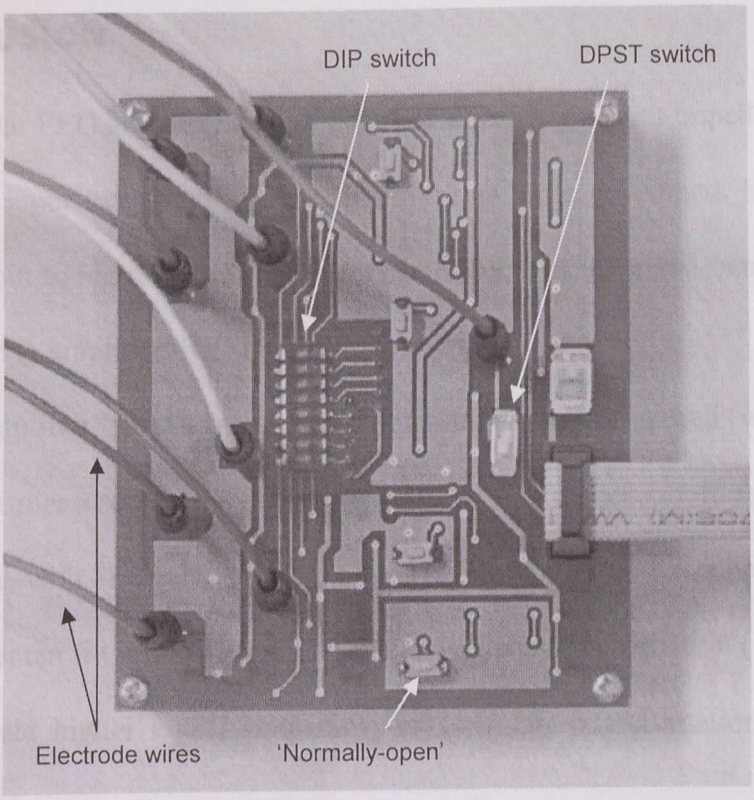


Figure 5.4: A photograph of the 'top' side of the amplifier board.

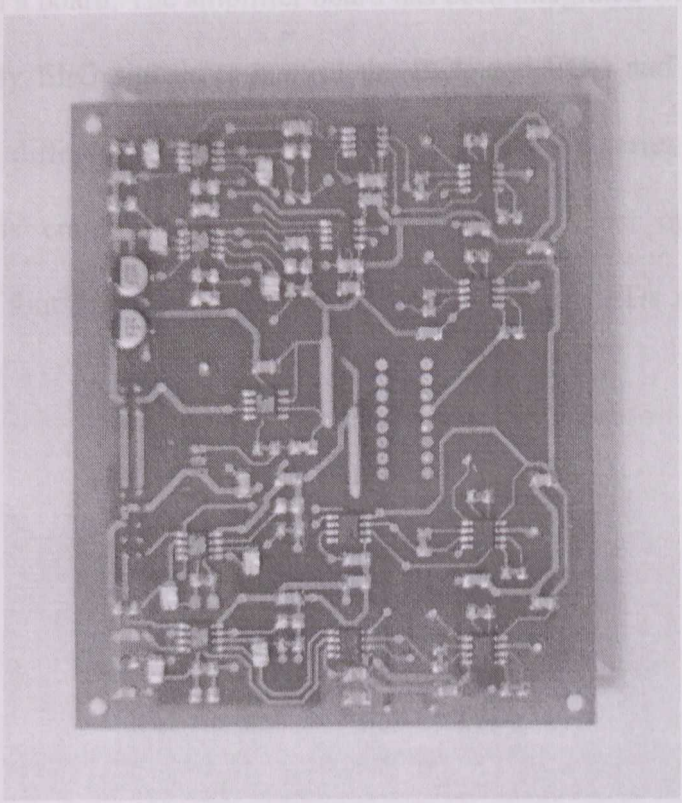


Figure 5.5: A photograph of the 'bottom' side of the amplifier board.

6 CONCLUSION

A bipolar EEG amplifier design with low noise, high input impedance, adequate differential dc input range and low power consumption is developed. High CMRR is achieved without tight resistor or capacitor matching. The gain and bandwidth can be easily modified to amplify other signals.

The amplifier specifications were measured and compared with calculated values. All the measured specifications, except for the higher cutoff frequency, were found to agree with the calculated values. Therefore, it can be concluded that the equations presented (in section 3.1), with the exception of the equation (3.4), which is used to calculate higher cutoff frequency, gives a fair approximation of the actual values.

Four channels (two EEG, an EOG and a chin EMG channel) with DRL circuit are constructed on a board. The amplifier board has been integrated with the UM-BCI to obtain and amplify EEG signals to control the BCI, and EOG and EMG for artifact rejection. Feature difference between two different motor imageries can be observed. This difference is employed to enable the subject to select options in a GUI corresponding to four prosthetic hand movements and four LEDs representing other devices.

Appendix A EQUATION DERIVATION

A.1 Differential gain

Assuming that all the op amps are ideal and summing currents at the inverting input terminal of OA1a and b in Figure 3.1, the input stage outputs, V_1 and V_2, are given by

$$V_1 = \left(1 + \frac{R_2}{R_1}\right) V_{IN1} - \frac{R_2}{R_1} V_{IN2}$$

$$V_2 = \left(1 + \frac{R_2}{R_1}\right) V_{IN2} - \frac{R_2}{R_1} V_{IN1}$$

The input stage outputs can also be expressed, in terms of the differential mode voltage, (V_{DM}) and the common mode voltage (V_{CM}) as

$$V_1 = \left(1 + \frac{2R_2}{R_1}\right)\left(\frac{-V_{DM}}{2}\right) + V_{CM}$$

$$V_2 = \left(1 + \frac{2R_2}{R_1}\right)\left(\frac{V_{DM}}{2}\right) + V_{CM}$$

Where $V_{DM} = V_{IN2} - V_{IN1}$, and

$$V_{CM} = (V_{IN2} + V_{IN1})/2$$

Subtracting V_1 from V_2 eliminates V_{CM} and leaves

$$V_2 - V_1 = \left(1 + \frac{2R_2}{R_1}\right) V_{DM} \qquad \text{(A.1)}$$

Applying voltage division at the inverting input of OA3 and OA4 and letting the potential at the inverting input equal that at the non-inverting input ($v_N = v_P$) gives

$$V_3 = \left(\frac{1 + sR_AC_A}{sR_AC_A}\right)\left(\frac{R_6}{R_5 + R_6}\right)\left(\frac{1 + sR_BC_B}{sR_BC_B}\right) V_{OUT} \qquad \text{(A.2)}$$

Using voltage division and superposition theorem to obtain the potential at the inverting and non-inverting inputs of OA2, and finally equating them ($v_N = v_P$) gives

$$\frac{R_4}{R_3 + R_4} V_2 = \frac{R_4}{R_3 + R_4} V_1 + \frac{R_3}{R_3 + R_4} V_3$$

$$V_2 - V_1 = \frac{R_3}{R_4} V_3$$

Substituting equations (A.1) and (A.2) into the above equation:

$$V_{OUT} = \left(1 + \frac{2R_2}{R_1}\right)\left(\frac{R_4}{R_3}\right)\left(1 + \frac{R_5}{R_6}\right)\left(\frac{sR_AC_A}{1 + sR_AC_A}\right)\left(\frac{sR_BC_B}{1 + sR_BC_B}\right) V_{DM}$$

(A.3)

A.2 Low pass frequency response

Summing currents at the inverting input and letting $v_{OUT} = a\ (v_P - v_N)$, the transfer function of the integrator used in the feedback loop, shown in Figure A.1a is

$$H(s) = V_B / V_A = \frac{a\ (1 + sRC)}{1 + sRC + asRC}$$

where a is the open loop gain of the op amp.

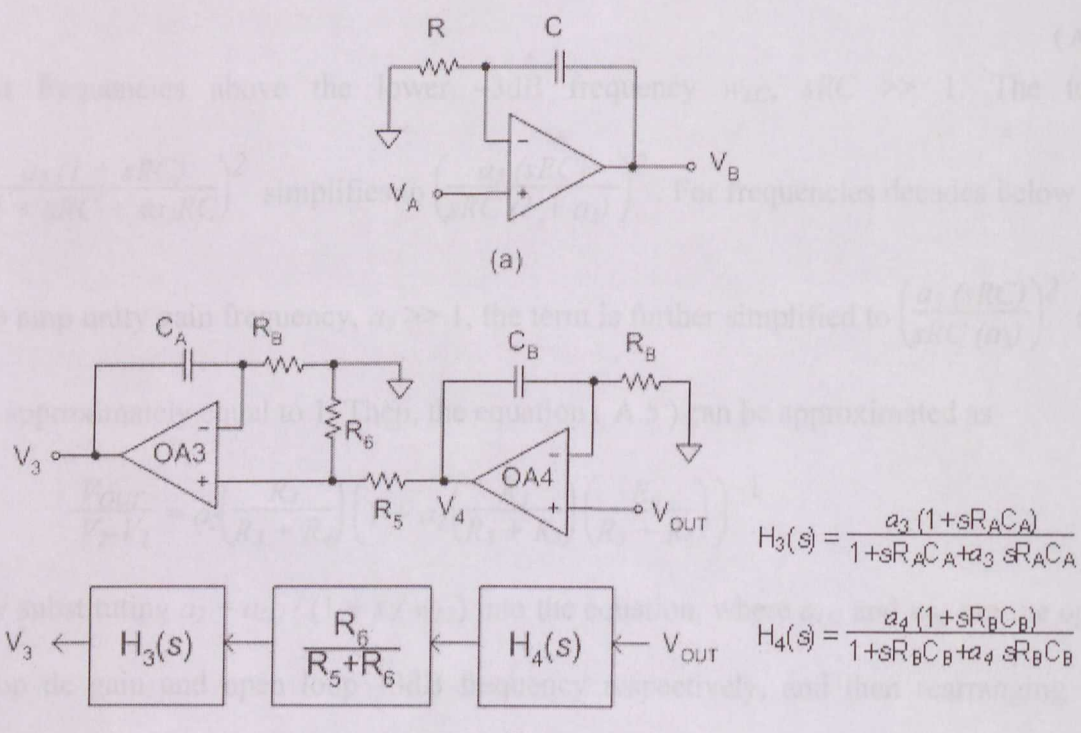


Figure A.1: Integrator feedback.

V_3 can be expressed in relation to V_{OUT} as

$$V_3 = H_3(s) \,.\, R_6 / (R_5 + R_6) \,.\, H_4(s)$$

$$V_3 = \left(\frac{a_3\,(1 + sR_AC_A)}{1 + sR_AC_A + sa_3R_AC_A}\right)\left(\frac{R_6}{R_5 + R_6}\right)\left(\frac{a_4\,(1 + sR_BC_B)}{1 + sR_BC_B + sa_4R_BC_B}\right) V_{OUT}$$

Since $R_A = R_B = R$ and $C_A = C_B = C$, and $a_3 = a_4$, the above equation can be rewritten as

$$V_3 = \left(\frac{R_6}{R_5 + R_6}\right)\left(\frac{a_3\,(1 + sRC)}{1 + sRC + sa_3RC}\right)^2 V_{OUT}$$

(A.4)

Deriving expression for voltage at the inverting and non-inverting input of OA2 and letting $V_{OUT} = a_2\,(V_p - V_n)$ yields

$$V_{OUT} = a_2\left(\frac{R_4}{R_3 + R_4}\,(V_2\text{-}V_1) - \frac{R_3}{R_3 + R_4}\,V_3\right)$$

Substituting equation (A.4) gives

$$V_{OUT}\left(1 + a_2\left(\frac{R_3}{R_3 + R_4}\right)\left(\frac{R_6}{R_5 + R_6}\right)\left(\frac{a_3\,(1 + sRC)}{1 + sRC + sa_3RC}\right)^2\right) = a_2\left(\frac{R_4}{R_3 + R_4}\right)(V_2\text{-}V_1)$$

(A.5)

At frequencies above the lower –3dB frequency w_{LC}, $sRC >> 1$. The term $\left(\frac{a_3\,(1 + sRC)}{1 + sRC + sa_3RC}\right)^2$ simplifies to $\left(\frac{a_3\,(sRC)}{sRC\,(1 + a_3)}\right)^2$. For frequencies decades below the op amp unity gain frequency, $a_3 >> 1$, the term is further simplified to $\left(\frac{a_3\,(sRC)}{sRC\,(a_3)}\right)^2$ and is approximately equal to 1. Then, the equation (A.5) can be approximated as

$$\frac{V_{OUT}}{V_2\text{-}V_1} = a_2\left(\frac{R_4}{R_3 + R_4}\right)\left(1 + a_2\left(\frac{R_3}{R_3 + R_4}\right)\left(\frac{R_6}{R_5 + R_6}\right)\right)^{-1}$$

By substituting $a_2 = a_{O2} / (1 + s / w_{b2})$ into the equation, where a_{O2} and w_{b2} are the open loop dc gain and open loop –3dB frequency respectively, and then rearranging the equation into the first order low pass response form $V_{OUT} / (V_2 - V_1) = A_O / (1 + s/w_{LP})$ where A_O is the dc gain and w_{LP} is the –3dB frequency,

$$\frac{V_{OUT}}{V_2\text{-}V_1} = \frac{a_{O2}\dfrac{R_4}{R_3 + R_4}}{1 + a_{O2}\dfrac{R_3}{R_3 + R_4}\dfrac{R_6}{R_5 + R_6}} \text{ X } \frac{1}{1 + \dfrac{s}{w_{b2}\left(1 + a_{O2}\dfrac{R_3}{R_3 + R_4}\dfrac{R_6}{R_5 + R_6}\right)}}$$

It can be readily seen that the –3dB frequency occurs at

$$w_{LP} = w_{b2}\left(1 + a_{O2}\frac{R_3}{R_3 + R_4}\frac{R_6}{R_5 + R_6}\right)$$

$$\approx w_{t2}\left(\frac{R_3}{R_3 + R_4}\right)\left(\frac{R_6}{R_5 + R_6}\right)$$

where w_{t2} is the unity gain bandwidth of OA2 and is equal to w_{b2} x a_{O2}. Rewriting the equation using f_{LP} and f_{t2}:

$$f_{LP} \approx f_{t2}\left(\frac{R_3}{R_3 + R_4}\right)\left(\frac{R_6}{R_5 + R_6}\right)$$

A.3 Bandwidth of difference amplifiers

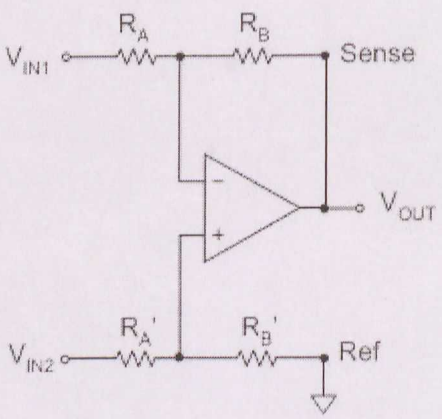


Figure A.2: A difference amplifier.

An expression for the bandwidth of difference amplifiers is obtained by assuming the that the op amp used is a compensated op amp having an open loop gain, a of a_O / (1 + s/w_b), where a_O and w_b are the open loop dc gain and –3dB frequency respectively.

Referring to Figure A.2, the relationship between V_{OUT} and $V_{IN2} - V_{IN1}$ is derived by summing currents at the inverting and non-inverting inputs of a difference amplifier with the sense input shorted to the output, and using the relationship $v_{OUT} = a\ (v_p - v_n)$

where a is the open loop gain, v_p and v_n are the voltage at the non-inverting and inverting input.

$$\frac{V_{OUT}}{V_{IN2}-V_{IN1}} = \frac{a\,R_B}{R_A + R_B + a\,R_A}$$

Substituting $a = a_O / (1 + s/w_b)$,

$$\frac{V_{OUT}}{V_{IN2}-V_{IN1}} = \frac{a_O\,R_B}{R_A + R_B + a_O\,R_A}\ X\ \frac{1}{1 + \dfrac{(s/w_b)\,(R_A + R_B)}{R_A + R_B + a_O\,R_A}}$$

From the above expression, the difference amplifier –3dB frequency is

$$w_{-3dB} = \frac{w_b\,(R_A+R_B+a_O R_A)}{R_A + R_B} \approx \frac{w_t\,R_A}{R_A + R_B}$$

In units of Hz,

$$f_{-3dB} \approx \frac{f_t\,R_A}{R_A + R_B}$$, where f_t is the unity gain frequency of the op amp in Hz.

Appendix B COMPUTER PROGRAMS

Program B.1: MATLAB program used produce the simulated bandpass response in Figure 4.3.

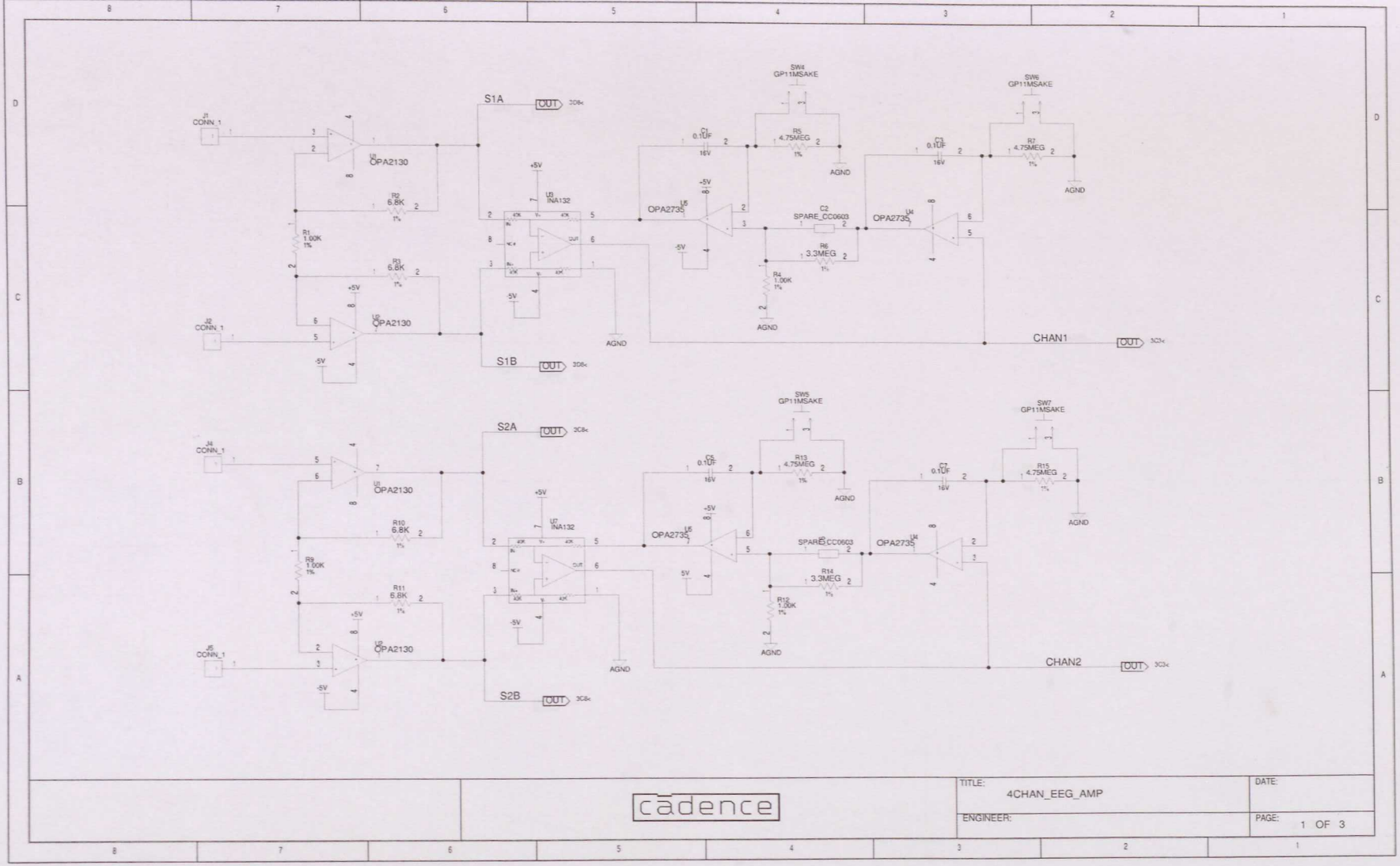
```
K=48177; %passband gain

%magnitude simulation - HPF
f1=0.1:0.1:5
fcHPF=0.509/1.554; %-3dB frequency = 0.509Hz
A1=(fcHPF./f1).^2+1;
mag1=K./A1;
mag1=dB(mag1);

%magnitude simulation - LPF
fcLPF=65.9; %-3dB frequency = 65.9Hz
f2=5:1:100;
A2=sqrt((f2/fcLPF).^2+1);
mag2=K./A2;
mag2=dB(mag2);

f3=100:100:3000;
A3=sqrt((f3/fcLPF).^2+1);
mag3=K./A3;
mag3=dB(mag3);

%Plotting gain vs frequency
semilogx(f1,mag1,'b--',f2,mag2,'b--',f3,mag3,'b--');
xlabel('Frequency (Hz)')
ylabel('Gain amplitude (dB)')
```

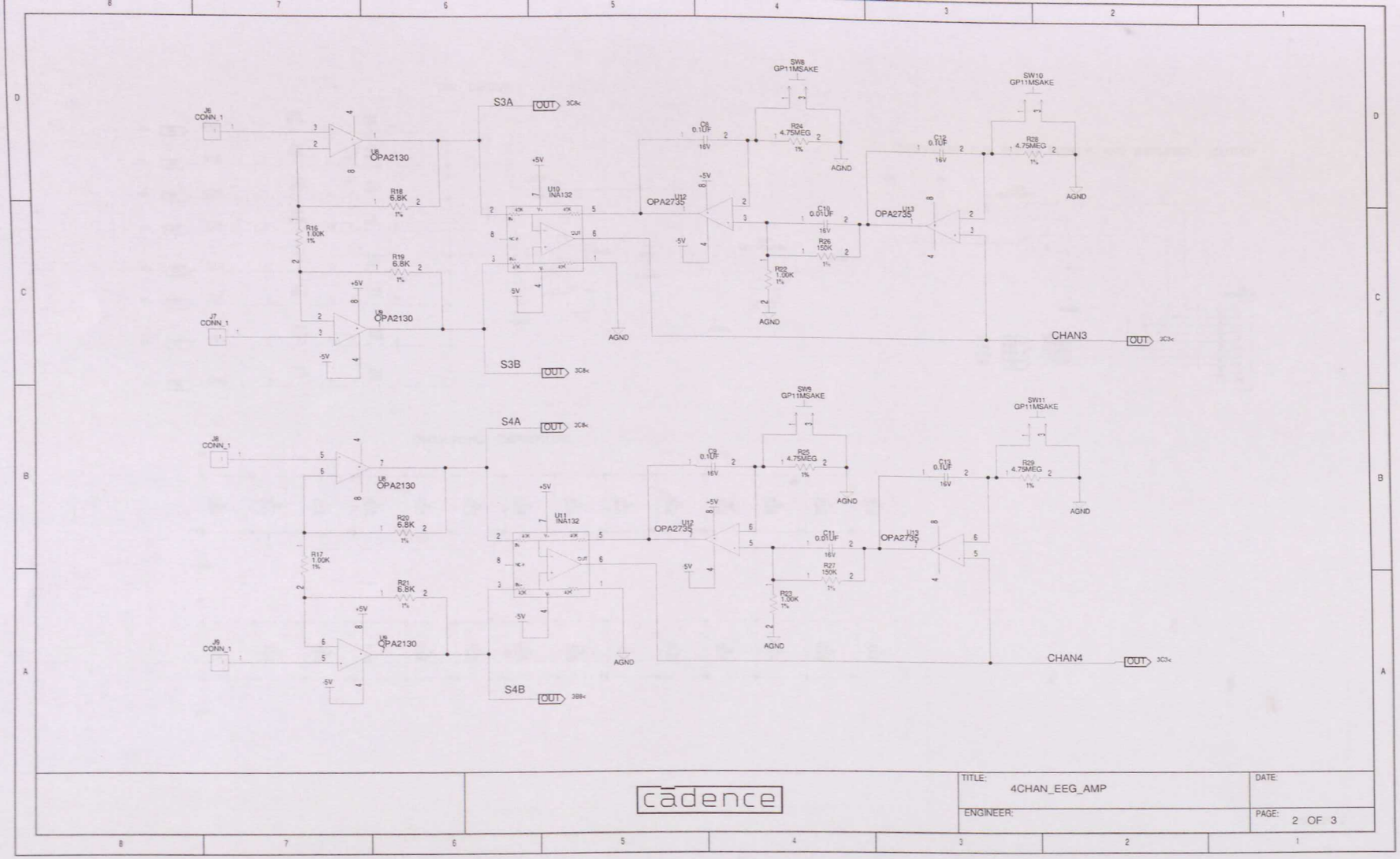
Program B.2: MATLAB program used to obtain the averaged power spectral plot in Figure 5.2.

```
function     y_mean=spectral(x,sampling_rate,step_size)
% 'x' is the time based data
% 'sampling_rate' is the number of samples in 'x' in a second
% 'step_size' is the window step size, set to equal the 'sampling_rate'
i=1;
lx=length(x);
max=floor((lx-sampling_rate)/step_size+1);

while(i<max+1)
  j=i*step_size-step_size+1;
  X=x(j:(j+sampling_rate-1));
  Fx=fft(X);
  PSD=Fx.*conj(Fx)/sampling_rate*2;
  k=1;
  while(k<sampling_rate/2)
    y(i,k)=PSD(k);
    k=k+1;
  end
  i=i+1;
end

y_mean = mean(y,1);
plot(2:45, y_mean(3:46));
```

Appendix C CIRCUIT SCHEMATIC

The full schematic of a four-channel amplifier (two EEG channels and two EOG and throat EMG) with DRL circuit is shown in the following 3 pages.


J1
CONN_1
U3
OPA2130
R2
6.8K
1%
R1
1.00K
1%
R3
6.8K
1%
J2
CONN_1
U6
OPA2130
+5V
-5V
S1A
OUT
3D8<
S1B
OUT
3D8<
U8
INA132
AGND
SW4
GP11MSAKE
C1
0.1UF
16V
R5
4.75MEG
1%
AGND
SW6
GP11MSAKE
C3
0.1UF
16V
R7
4.75MEG
1%
AGND
U5
OPA2735
C2
SPARE_CC0603
R6
3.3MEG
1%
R4
1.00K
1%
AGND
U4
OPA2735
CHAN1
OUT
3C3<
J4
CONN_1
U1
OPA2130
R10
6.8K
1%
R9
1.00K
1%
R11
6.8K
1%
J5
CONN_1
U2
OPA2130
+5V
-5V
S2A
OUT
3C8<
S2B
OUT
3C8<
U7
INA132
AGND
SW5
GP11MSAKE
C6
0.1UF
16V
R13
4.75MEG
1%
AGND
SW7
GP11MSAKE
C7
0.1UF
16V
R15
4.75MEG
1%
AGND
U5
OPA2735
SPARE_CC0603
R14
3.3MEG
1%
R12
1.00K
1%
AGND
U4
OPA2735
CHAN2
OUT
3C3<
cadence
TITLE:
4CHAN_EEG_AMP
DATE:
ENGINEER:
PAGE:
1 OF 3



	cadence	TITLE: 4CHAN_EEG_AMP	DATE:
		ENGINEER:	PAGE: 2 OF 3

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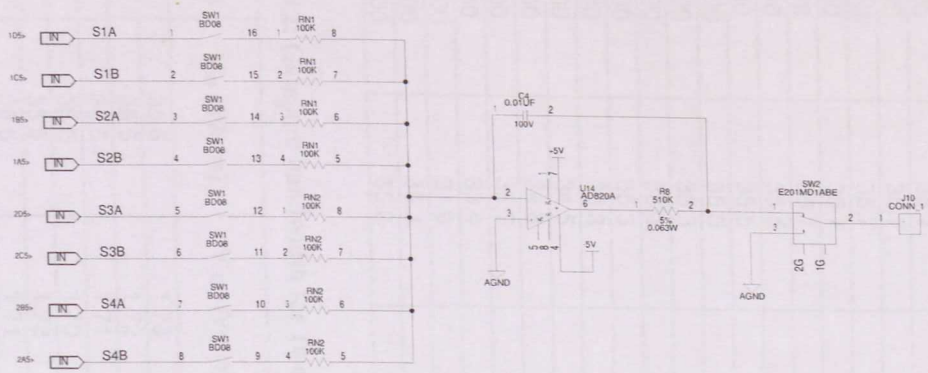
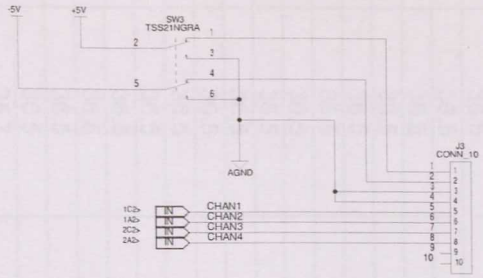
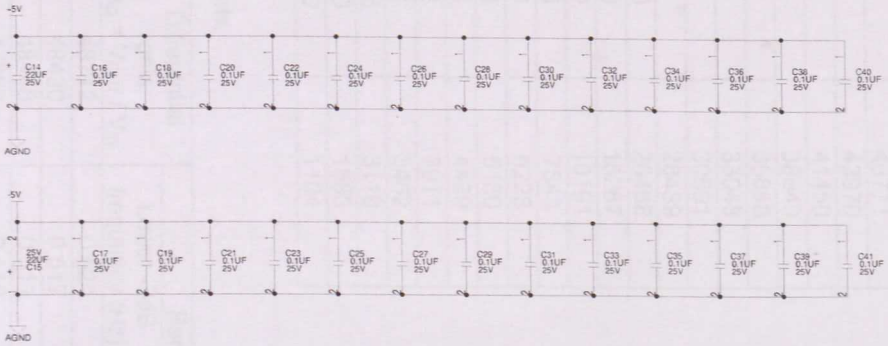
DRL CIRCUIT



CONNECTOR FOR POWER SUPPLY AND AMPLIFIER OUTPUT



DECOUPLING CAPACITORS



	cadence	TITLE: 4CHAN_EEG_AMP	DATE:
		ENGINEER:	PAGE: 3 OF 3

Appendix D EXPERIMENTAL DATA

Table D.1: Gain magnitude response of one channel.

Frequency(Hz)	V_{IN} (μVrms)	V_{OUT} (Vrms)	Differential gain, $A_D = V_{OUT} / V_{IN}$
0.1	36.5	0.150	4110
0.2	36.5	0.449	12317
0.3	36.5	0.728	19962
0.4	36.5	1.00	27544
0.5	36.5	1.15	31617
0.6	36.5	1.27	34721
0.7	36.5	1.39	38018
0.8	36.5	1.44	39570
0.9	36.5	1.48	40734
1	36.5	1.53	41898
2	36.5	1.68	46165
3	36.5	1.70	46553
4	36.5	1.74	47717
5	36.5	1.74	47717
6	36.5	1.74	47717
7	36.5	1.74	47717
8	36.5	1.74	47717
9	36.5	1.74	47717
10	36.5	1.74	47717
20	35.7	1.67	46771
30	35.7	1.57	43970
40	35.7	1.48	41450
50	35.7	1.38	38649
60	35.7	1.28	35848
70	35.7	1.18	33048
80	35.5	1.09	30691
90	35.5	1.01	28439
100	35.5	0.940	26468
200	35.3	0.540	15287
300	35.3	0.360	10191
400	35.3	0.270	7643
500	35.3	0.220	6228
600	34.5	0.178	5160
700	34.8	0.156	4489
800	33.7	0.132	3911
900	33.4	0.116	3462
1000	31.9	0.0995	3119
2000	35.3	0.0560	1585
3000	35.3	0.0390	1104

Table D.2: Gain and bandwidth for 10 channels.

Channel	V_{IN} (μVrms)	V_{OUT} (Vrms)	Differential gain, $A_D = V_{OUT} / V_{IN}$	Bandwidth	
				Lower -3dB frequency (Hz)	Upper -3dB frequency (Hz)
1	35.5	1.73	48712	0.524	65.6
2	35.5	1.72	48430	0.517	66.2
3	35.5	1.71	48148	0.511	65.4
4	35.5	1.70	47867	0.510	66.8
5	35.5	1.72	48430	0.486	65.6
6	35.5	1.71	48148	0.513	66.2
7	35.5	1.70	47867	0.512	66.2
8	35.5	1.70	47867	0.522	65.7
9	35.5	1.70	47867	0.505	66.0
10	35.5	1.72	48430	0.486	65.5
MEAN			48177	0.509	65.9
MAX DEVIATION FROM MEAN			-535, 310	-0.015, 0.023	-0.9, 0.5

Table D.3: Stability of gain and bandwidth during continuous operation for 2 channels.

Channel 1					
Time	V_{IN} (μVrms)	V_{OUT} (Vrms)	Differential gain, $A_D = V_{OUT} / V_{IN}$	Bandwidth	
				Lower -3dB frequency (Hz)	Upper -3dB frequency (Hz)
27-May-2005					
08:40	36.25	1.77	48956	0.539	63.7
09:10	36.25	1.77	48859	0.513	63.8
09:40	36.25	1.77	48956	0.548	64.3
10:10	36.25	1.76	48566	0.530	63.2
10:40	36.25	1.76	48566	0.537	64.8
11:10	36.25	1.75	48371	0.519	65.9
11:40	36.25	1.75	48371	0.520	64.0
12:10	36.25	1.75	48371	0.536	66.3
12:40	36.25	1.77	48859	0.561	62.4
MEAN			48653	0.534	64.3
MAX DEVIATION FROM MEAN			-282, 303	-0.027, 0.021	-1.9, 2.0
28-May-2005					
09:15	36.25	1.76	48566	0.538	63.4

Channel 2					
Time	V_{IN} (μVrms)	V_{OUT} (Vrms)	Differential gain, $A_D = V_{OUT} / V_{IN}$	Bandwidth	
				Lower -3dB frequency (Hz)	Upper -3dB frequency (Hz)
27-May-2005					
08:40	36.25	1.76	48566	0.519	66.7
09:10	36.25	1.76	48566	0.537	64.9
09:40	36.25	1.75	48371	0.517	65.9
10:10	36.25	1.76	48566	0.529	64.3
10:40	36.25	1.76	48664	0.543	65.8
11:10	36.25	1.75	48371	0.521	67.2
11:40	36.25	1.74	47981	0.551	66.5
12:10	36.25	1.74	47981	0.546	67.7
12:40	36.25	1.76	48566	0.534	65.5
MEAN			48404	0.533	66.1
MAX DEVIATION FROM MEAN			-423, 260	-0.016, 0.018	-1.8, 1.6
28-May-2005					
09:15	36.25	1.75	48176	0.528	67.2

Table D.4: Gain and bandwidth in 5 different days.

Channel 1					
Date	V_{IN} (μVrms)	V_{OUT} (Vrms)	Differential gain, $A_D = V_{OUT} / V_{IN}$	Bandwidth	
				Lower -3dB frequency (Hz)	Upper -3dB frequency (Hz)
24-May-05	36.25	1.77	48956	0.539	63.7
26-May-05	36.52	1.77	48400	0.533	63.3
27-May-05	36.25	1.77	48956	0.539	63.7
28-May-05	36.25	1.76	48566	0.538	63.4
29-May-05	36.25	1.77	48761	0.537	63.2
MEAN			48728	0.537	63.5
MAX DEVIATION FROM MEAN			-328, 228	-0.004,0.002	-0.3, 0.2

Channel 2					
Date	V_{IN} (μVrms)	V_{OUT} (Vrms)	Differential gain, $A_D = V_{OUT} / V_{IN}$	Bandwidth	
				Lower -3dB frequency (Hz)	Upper -3dB frequency (Hz)
24-May-05	36.25	1.75	48371	0.517	65.9
26-May-05	36.52	1.75	48013	0.535	65.7
27-May-05	36.25	1.76	48566	0.519	66.7
28-May-05	36.25	1.75	48176	0.528	67.2
29-May-05	36.25	1.74	47981	0.532	65.9
MEAN			48221	0.526	66.3
MAX DEVIATION FROM MEAN			-240, 345	-0.009, 0.009	-0.6,0.9

Table D.5: Common mode rejection ratio (CMRR) for 10 channels.

Channel	Differential mode			Common mode			CMRR = A_D / A_C (dB)
	V_{IN} (μVrms)	V_{OUT} (Vrms)	Differential gain, $A_D = V_{OUT} / V_{IN}$	V_{IN} (Vrms)	V_{OUT} (Vrms)	Common mode gain, $A_C = V_{OUT} / V_{IN}$	
1	54.23	2.100	38726	1.970	0.191	0.0970	112.0
2	35.61	1.360	38191	1.532	0.287	0.1873	106.2
3	35.61	1.357	38107	1.532	0.430	0.2807	102.7
4	50.60	1.950	38538	1.970	0.240	0.1218	110.0
5	31.89	1.233	38667	1.563	0.347	0.2220	104.8
6	31.89	1.220	38260	1.563	0.050	0.0320	121.6
7	41.53	1.594	38382	1.761	0.197	0.1119	110.7
8	41.53	1.600	38527	1.761	0.356	0.2022	105.6
9	41.53	1.590	38286	1.761	0.246	0.1397	108.8
10	41.53	1.600	38527	1.761	0.206	0.1170	110.4
						MINIMUM	102.7

Table D.6: Stability of CMRR during continuous operation for 2 channels.

Channel 3							
Date/ Time	Differential mode			Common mode			CMRR = A_D / A_C (dB)
	V_{IN} (μVrms)	V_{OUT} (Vrms)	Differential gain, $A_D = V_{OUT} / V_{IN}$	V_{IN} (Vrms)	V_{OUT} (Vrms)	Common mode gain, $A_C = V_{OUT} / V_{IN}$	
27-May-2005							
9:00	50.18	1.927	38409	1.898	0.379	0.1997	105.7
9:30	49.40	1.881	38086	1.851	0.134	0.0726	114.4
10:00	50.33	1.928	38312	1.863	0.407	0.2185	104.9
10:30	48.90	1.881	38459	1.866	0.415	0.2222	104.8
11:00	48.96	1.795	36671	1.823	0.407	0.2231	104.3
11:30	50.20	1.928	38407	1.861	0.428	0.2300	104.5
12:00	43.29	1.658	38311	1.929	0.432	0.2241	104.7
12:30	48.44	1.858	38348	1.886	0.414	0.2193	104.9
13:00	48.77	1.876	38462	1.832	0.428	0.2338	104.3
						MIN	104.3
						MEAN	105.8
						MAX DEVIATION FROM MEAN	-1.5, 8.6
28-May-2005							
9:30	48.17	1.848	38354	1.873	0.424	0.2262	104.6

Channel 4							
Time	Differential mode			Common mode			CMRR = A_D / A_C (dB)
	V_{IN} (μVrms)	V_{OUT} (Vrms)	Differential gain, $A_D = V_{OUT} / V_{IN}$	V_{IN} (Vrms)	V_{OUT} (Vrms)	Common mode gain, $A_C = V_{OUT} / V_{IN}$	
27-May-2005							
9:00	50.18	1.909	38043	1.898	0.241	0.1272	109.5
9:30	49.40	1.877	37992	1.851	0.154	0.0834	113.2
10:00	50.33	1.925	38246	1.863	0.221	0.1186	110.2
10:30	48.90	1.875	38350	1.866	0.220	0.1181	110.2
11:00	48.96	1.853	37849	1.823	0.162	0.0890	112.6
11:30	48.44	1.851	38204	1.886	0.206	0.1094	110.9
12:00	48.77	1.870	38339	1.832	0.202	0.1104	110.8
12:30	43.29	1.657	38280	1.929	0.216	0.1120	110.7
13:00	49.11	1.873	38139	1.890	0.223	0.1180	110.2
						MIN	109.5
						MEAN	110.9
						MAX DEVIATION FROM MEAN	-0.7, 2.3
28-May-2005							
9:30	48.17	1.851	38423	1.873	0.216	0.1153	110.5

Table D.7: CMRR in 5 different days.

Channel 3							
Date	Differential mode			Common mode			CMRR = A_D / A_C (dB)
	V_{IN} (μVrms)	V_{OUT} (Vrms)	Differential gain, $A_D = V_{OUT} / V_{IN}$	V_{IN} (Vrms)	V_{OUT} (Vrms)	Common mode gain, $A_C = V_{OUT} / V_{IN}$	
24-May-05	35.88	1.357	37818	1.532	0.430	0.2807	102.6
26-May-05	49.40	1.898	38424	1.880	0.451	0.2399	104.1
27-May-05	50.18	1.927	38409	1.898	0.379	0.1997	105.7
28-May-05	48.17	1.848	38354	1.873	0.424	0.2262	104.6
29-May-05	48.10	1.850	38470	1.880	0.411	0.2184	104.9
						MIN	102.6
						MEAN	104.4
						MAX DEVIATION FROM MEAN	-1.8, 1.3

Channel 4							
Date	Differential mode			Common mode			CMRR = A_D / A_C (dB)
	V_{IN} (μVrms)	V_{OUT} (Vrms)	Differential gain, $A_D = V_{OUT} / V_{IN}$	V_{IN} (Vrms)	V_{OUT} (Vrms)	Common mode gain, $A_C = V_{OUT} / V_{IN}$	
24-May-05	50.99	1.950	38246	1.970	0.240	0.1218	109.9
26-May-05	49.40	1.887	38201	1.880	0.227	0.1207	110.0
27-May-05	50.18	1.909	38043	1.898	0.241	0.1272	109.5
28-May-05	48.17	1.851	38423	1.873	0.216	0.1153	110.5
29-May-05	48.10	1.841	38284	1.880	0.301	0.1601	107.6
						MIN	107.6
						MEAN	109.5
						MAX DEVIATION FROM MEAN	-1.9, 1.0

Table D.8: Maximum differential dc and ac input range.

	Maximum differential dc input (mV)		Maximum differential ac input (μVp-p)
	Positive	Negative	
1	342.3	-342.1	177
2	340.8	-342.3	171
3	341.4	-341.3	179
4	341.6	-343.1	175
5	341.3	-341.9	173
MINIMUM	340.8	-341.3	171

Appendix E EEG RECORDED DURING BCI SESSIONS

The following figures show segments of recording and the averaged power spectral plot of EEG acquired from different subjects and during separate training sessions using the EEG amplifier built.

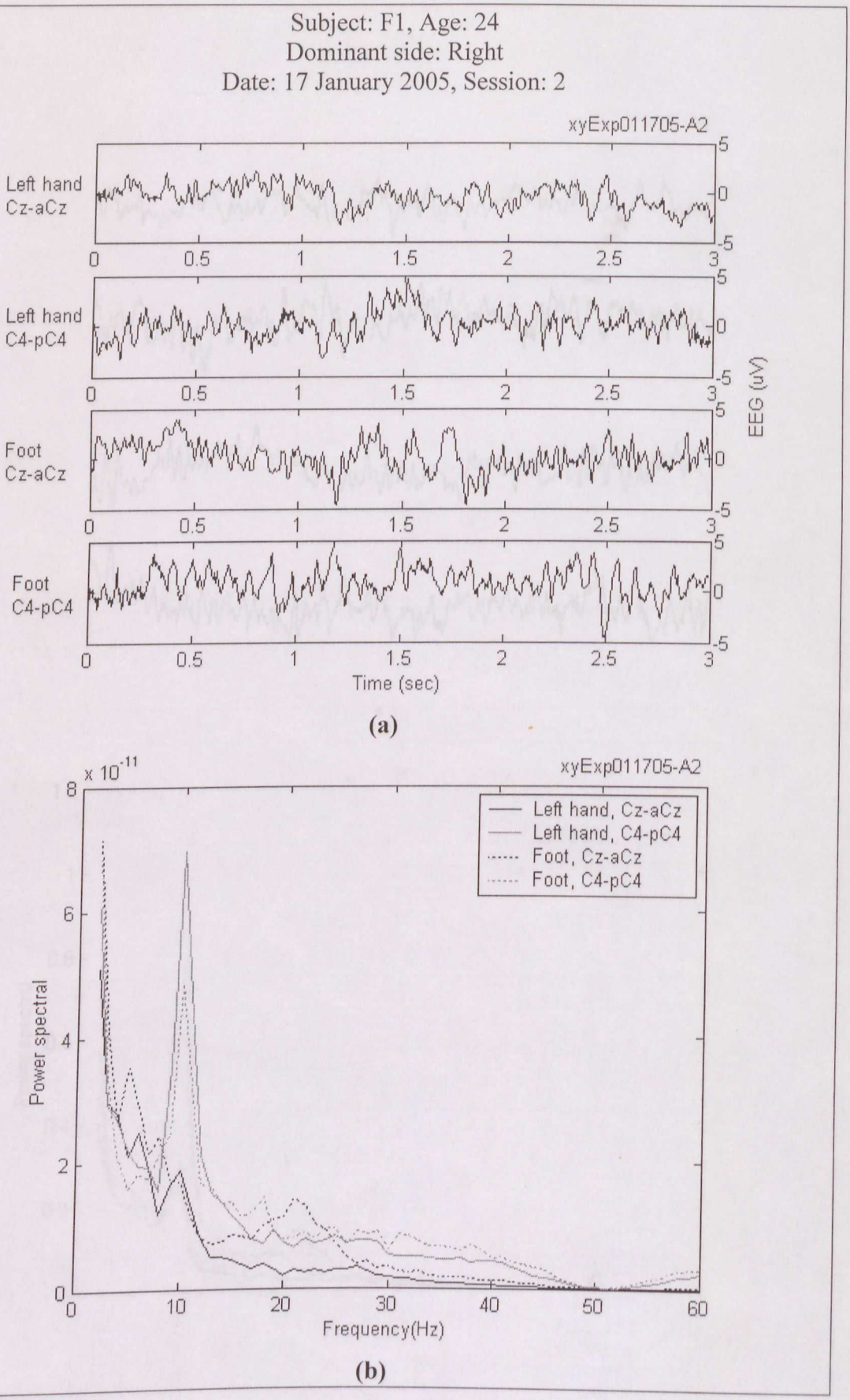


Figure E.1: (a) A segment of the EEG acquired; (b) The averaged power spectral plot of EEG signals recorded from subject F1 during the 2nd session on 17 January 2005.

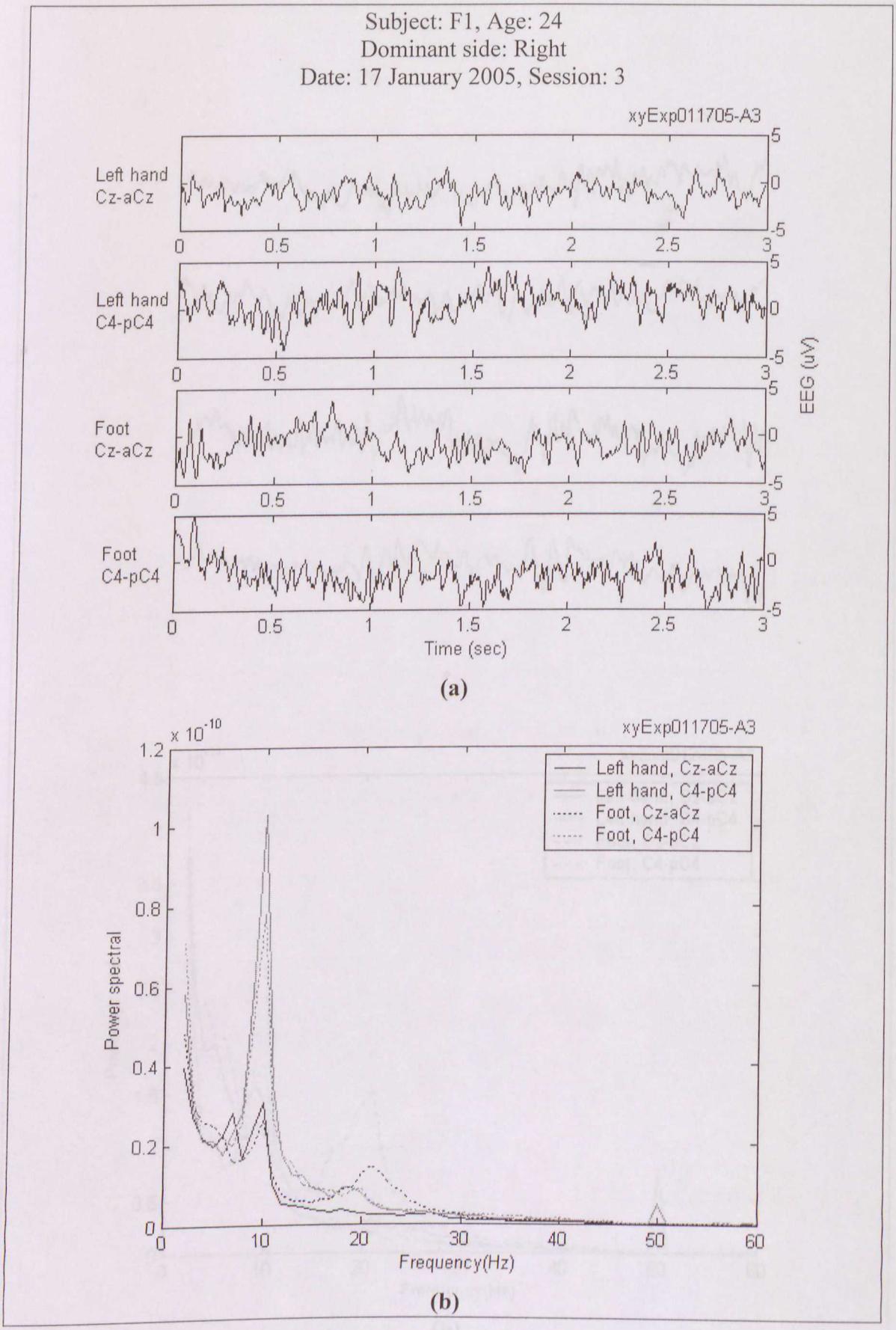


Figure E.2: (a) A segment of the EEG acquired; (b) The averaged power spectral plot of EEG signals recorded from subject F1 during the 3rd session on 17 January 2005.

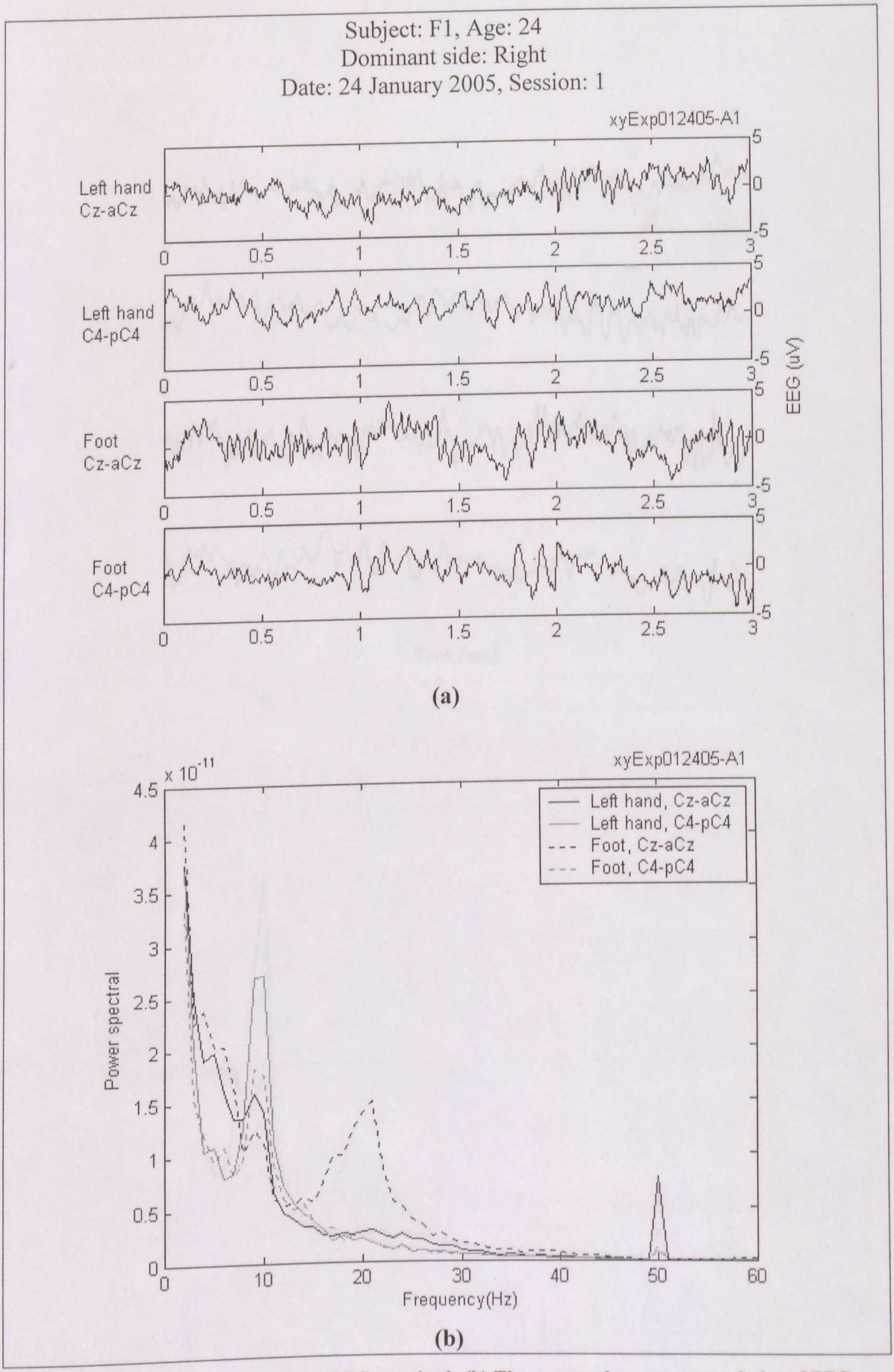


Figure E.3: (a) A segment of the EEG acquired; (b) The averaged power spectral plot of EEG signals recorded from subject F1 during the 1st session on 24 January 2005.

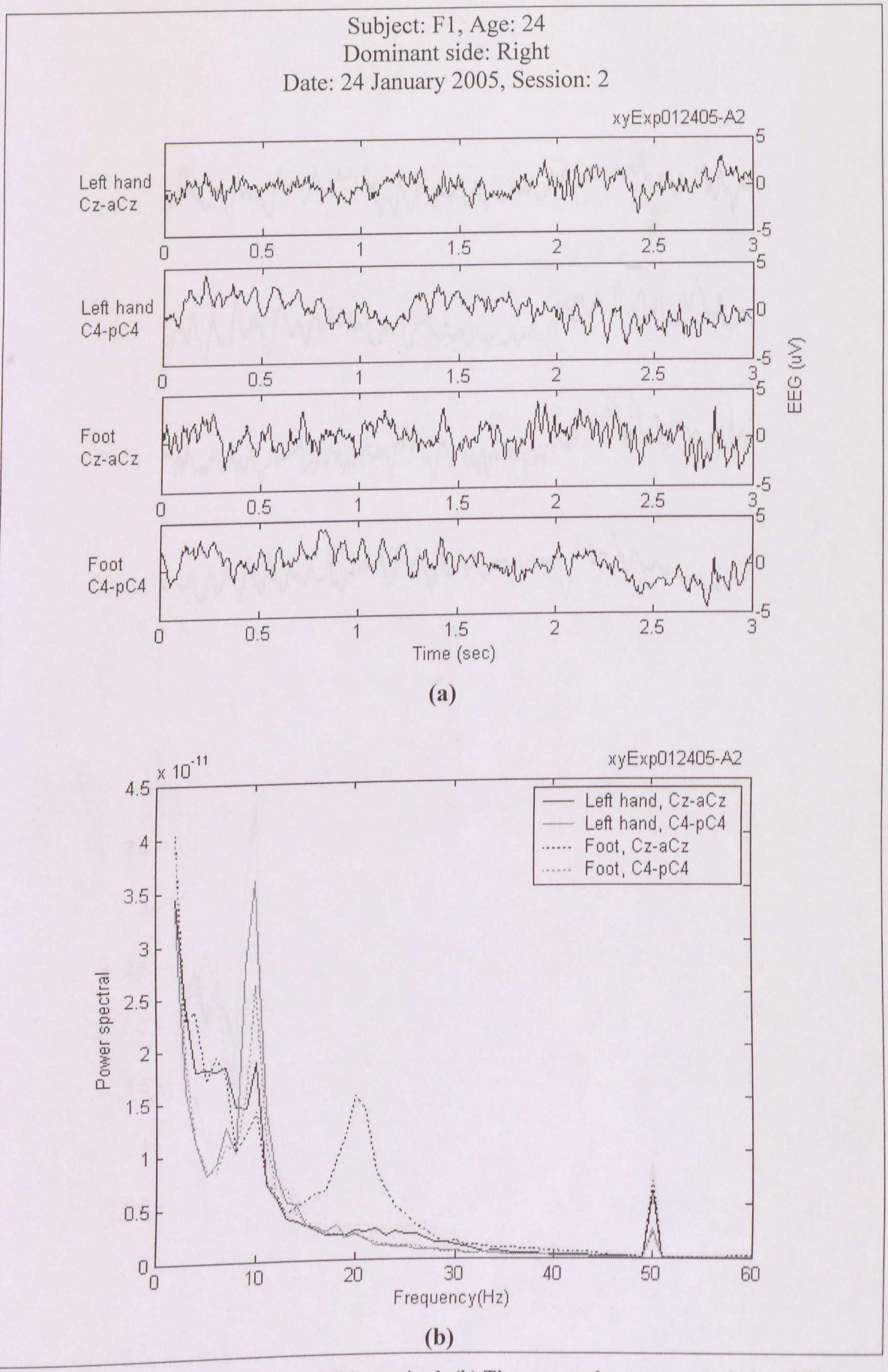


Figure E.4: (a) A segment of the EEG acquired; (b) The averaged power spectral plot of EEG signals recorded from subject F1 during the 2nd session on 24 January 2005.

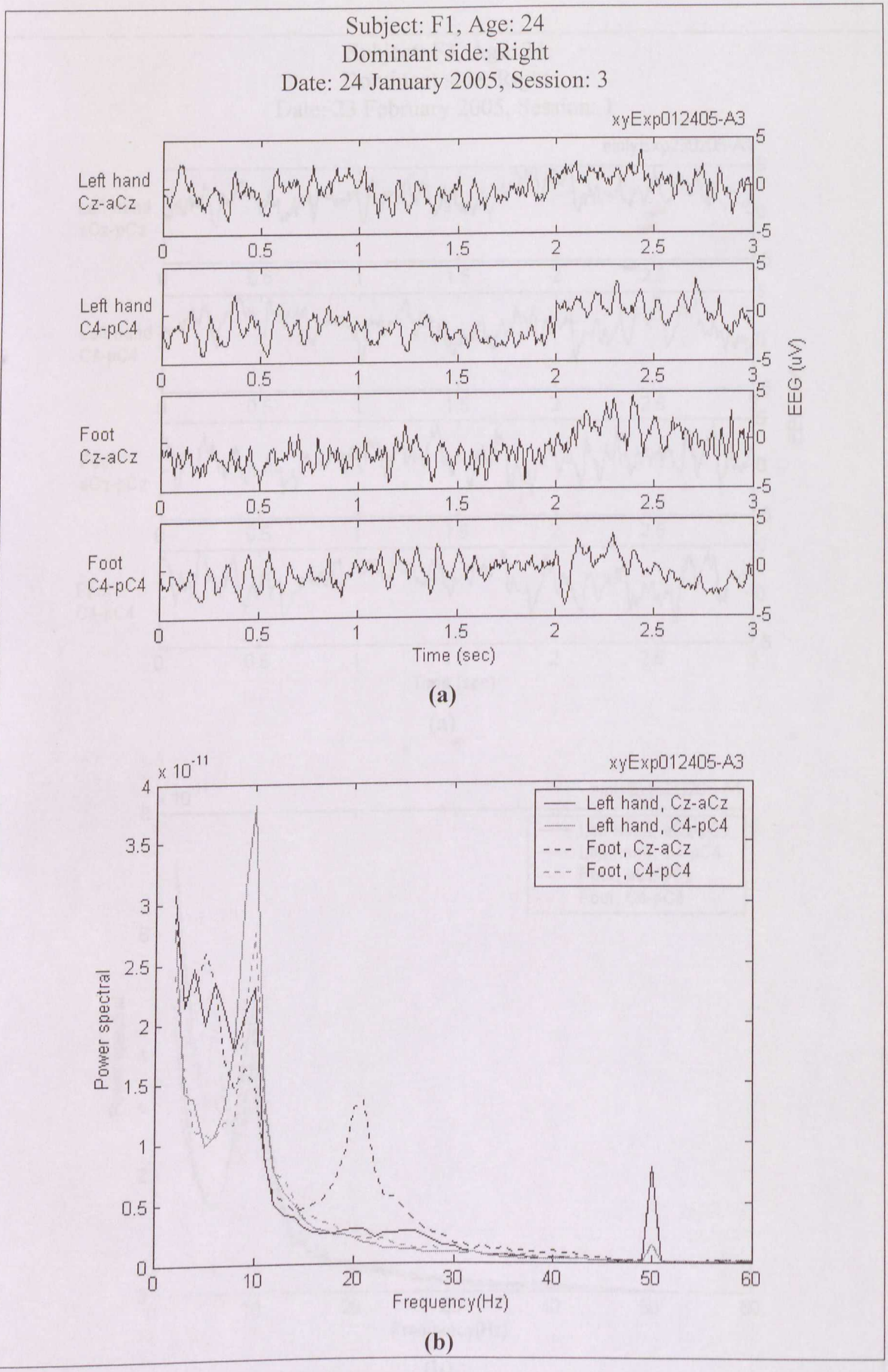
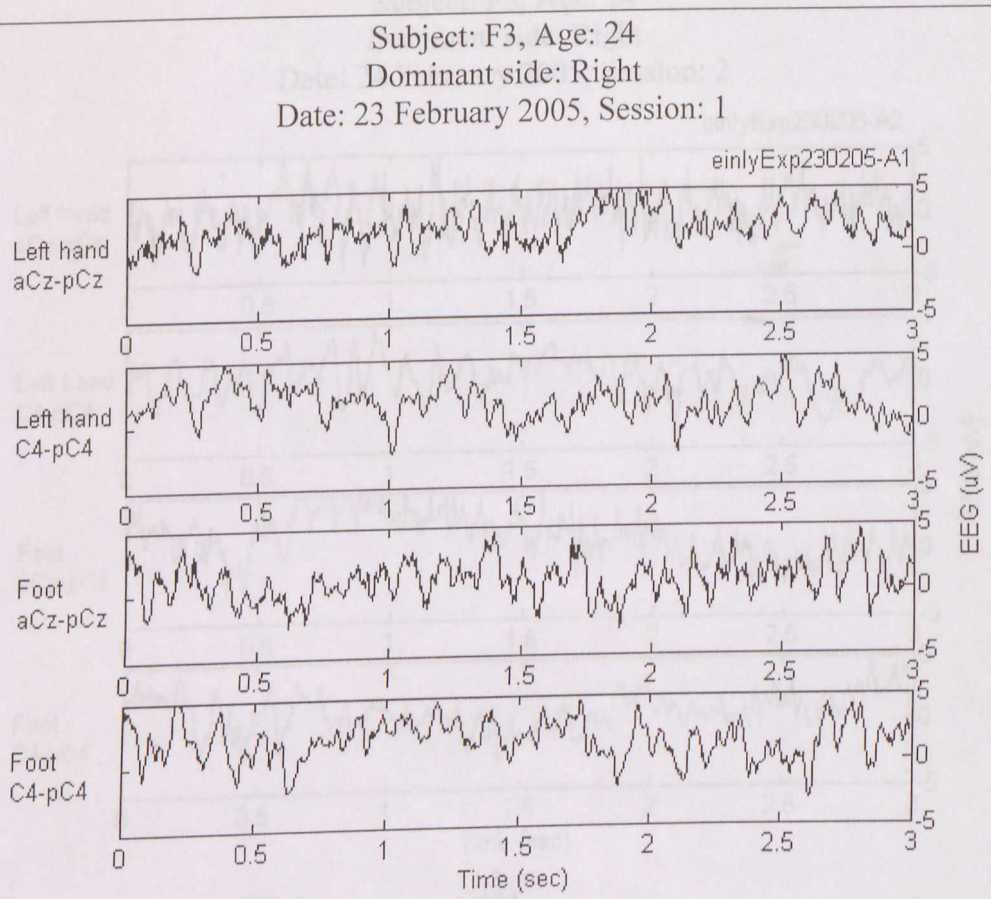
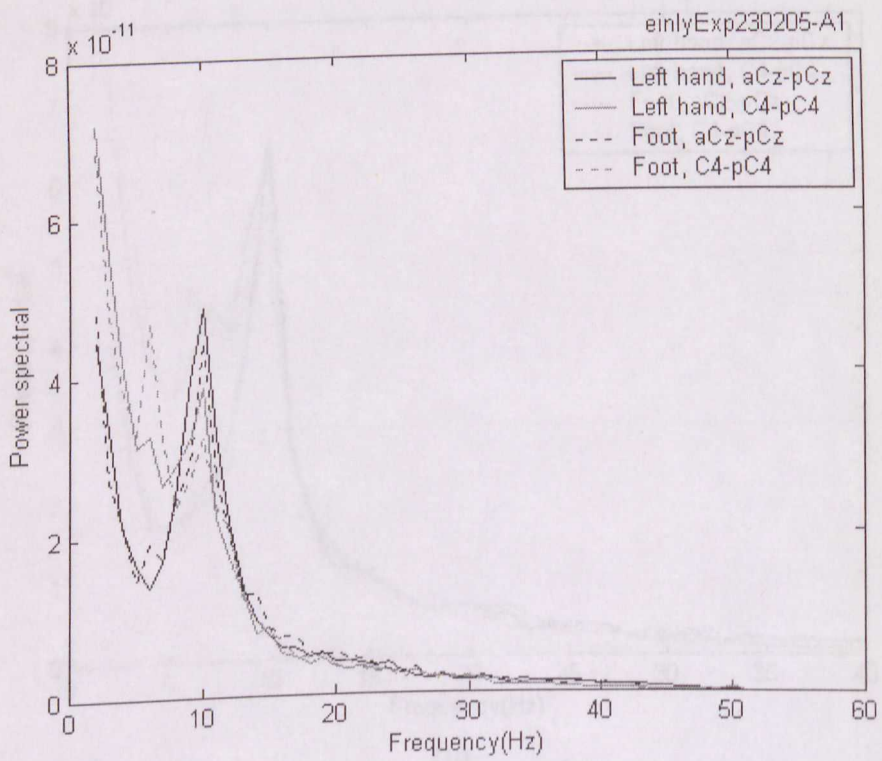


Figure E.5: (a) A segment of the EEG acquired; (b) The averaged power spectral plot of EEG signals recorded from subject F1 during the 3rd session on 24 January 2005.



(a)



(b)

Figure E.6: (a) A segment of the EEG acquired; (b) The averaged power spectral plot of EEG signals recorded from subject F3 during the 1st session on 23 February 2005.

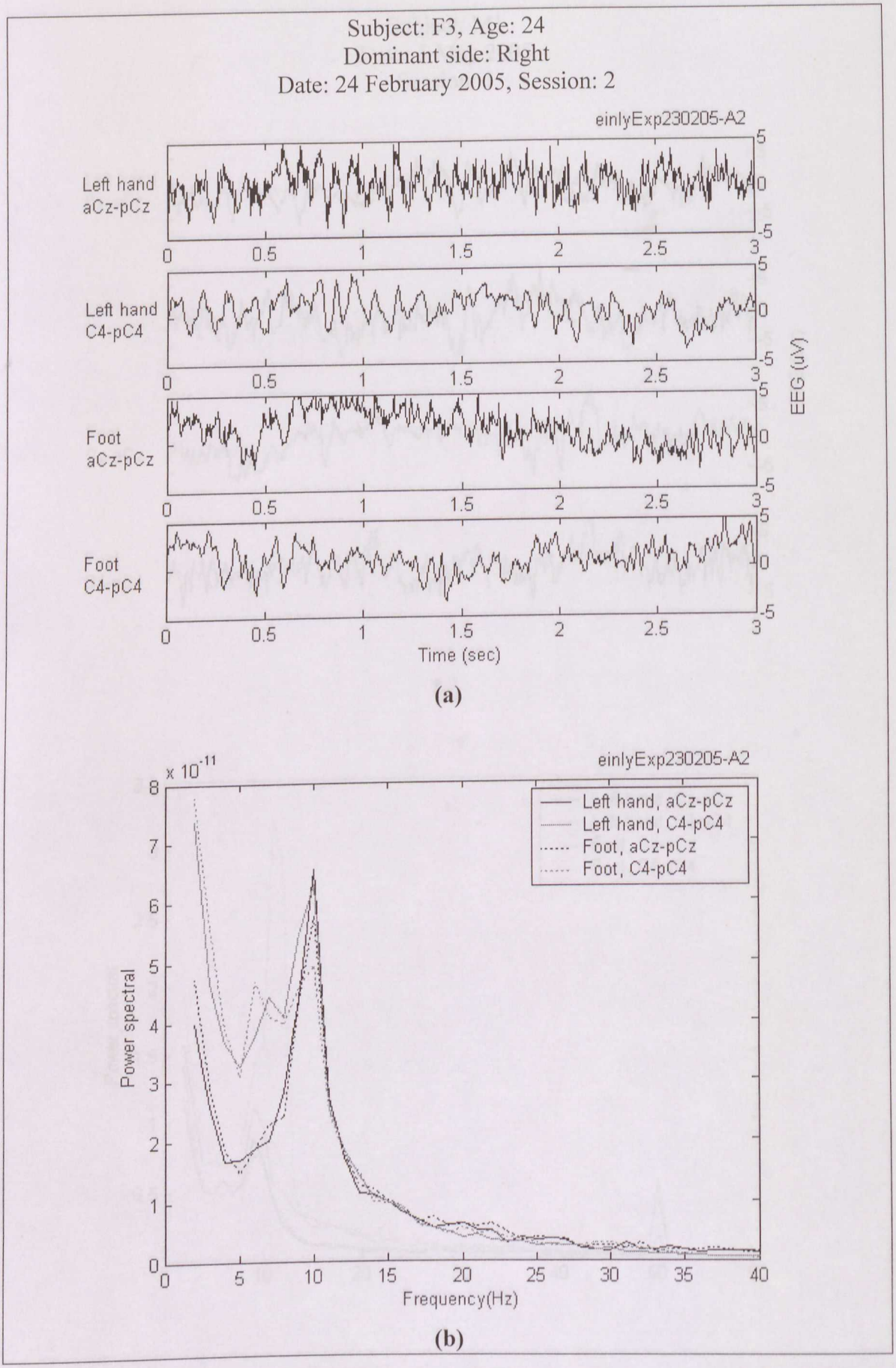


Figure E.7: (a) A segment of the EEG acquired; (b) The averaged power spectral plot of EEG signals recorded from subject F1 during the 2nd session on 23 February 2005.

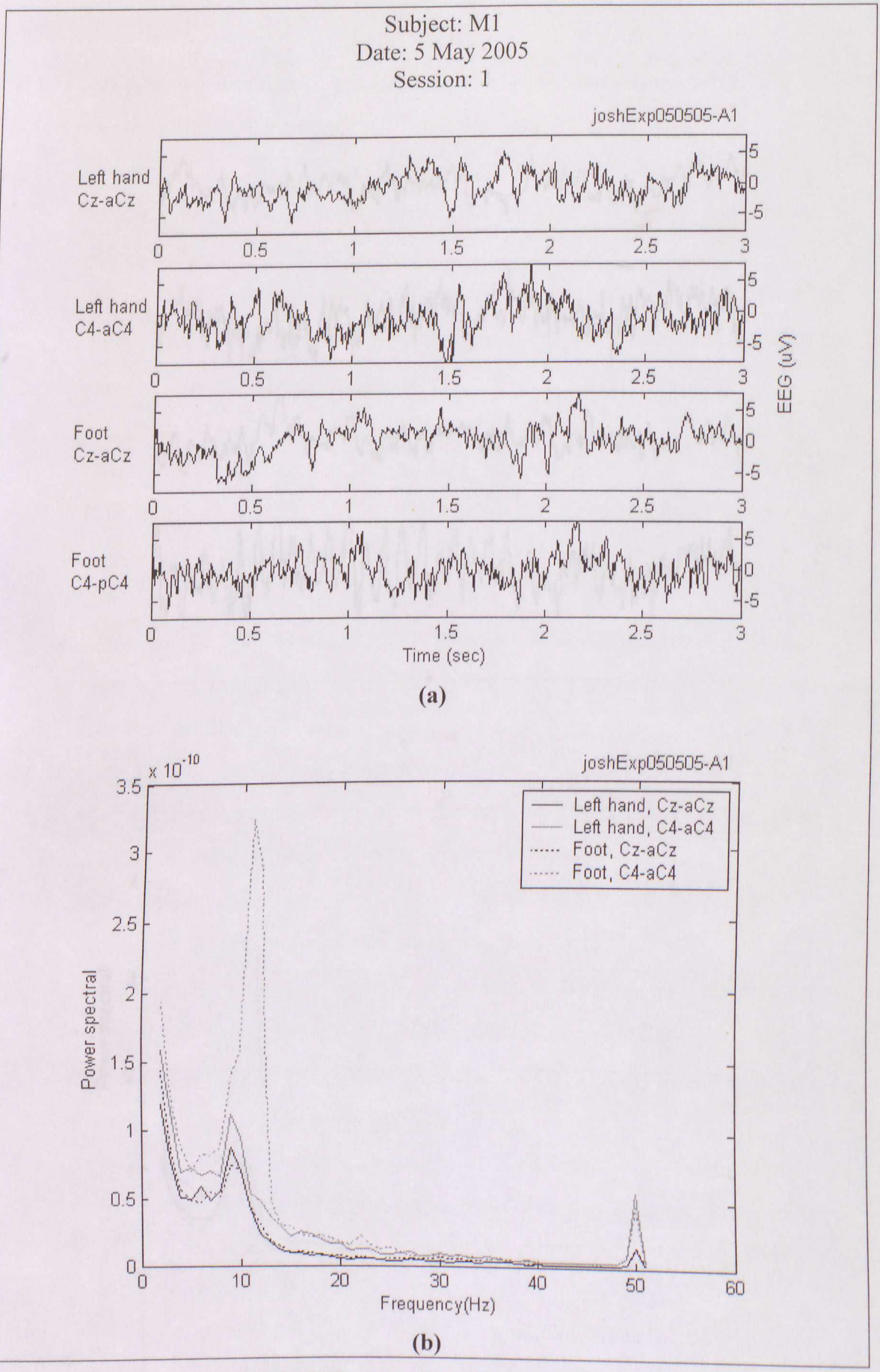


Figure E.8: (a) A segment of the EEG acquired; (b) The averaged power spectral plot of EEG signals recorded from subject M1 during the 1st session on 5 May 2005.

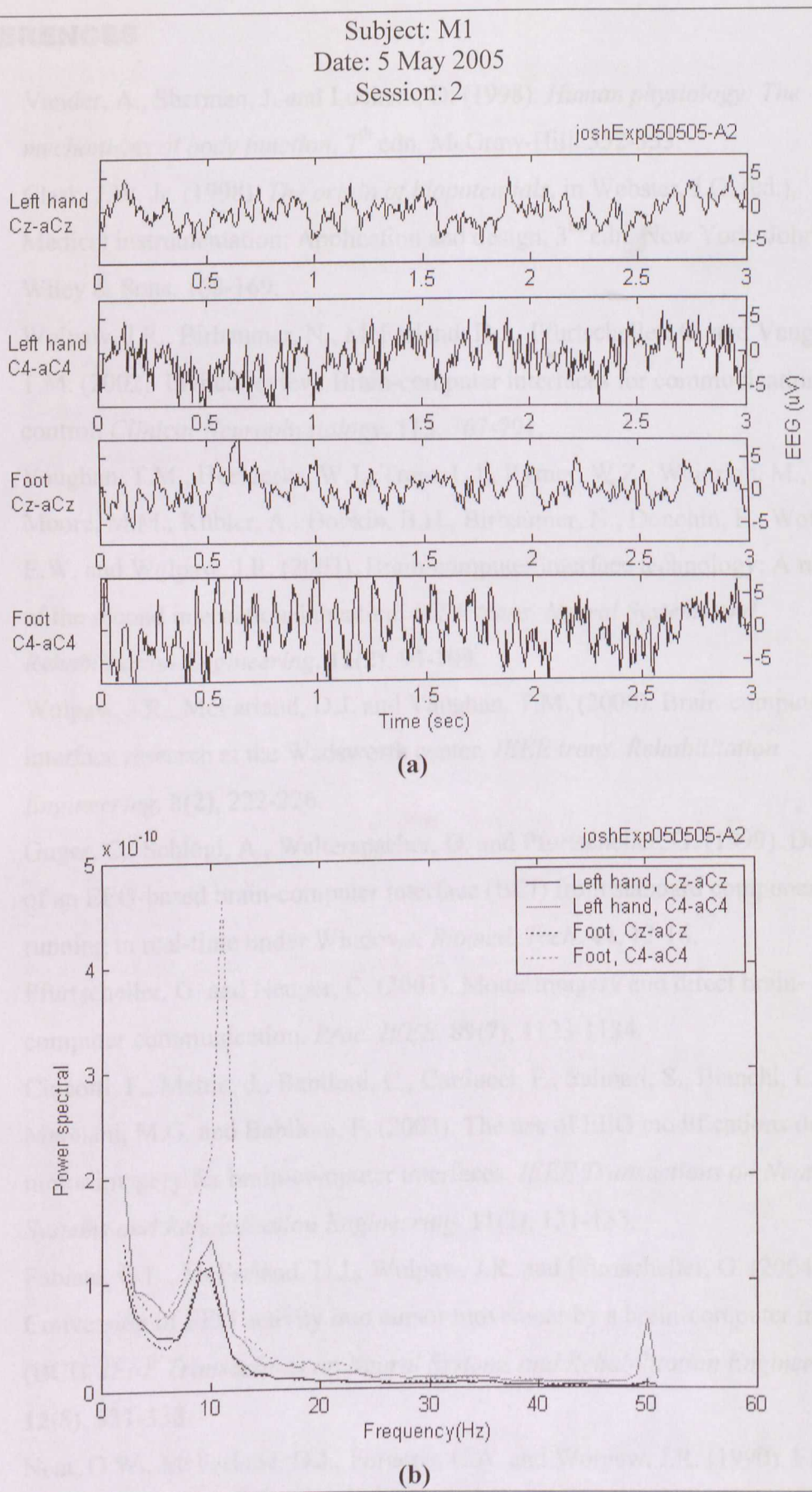


Figure E.9: (a) A segment of the EEG acquired; (b) The averaged power spectral plot of EEG signals recorded from subject M1 during the 1st session on 5 May 2005.

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